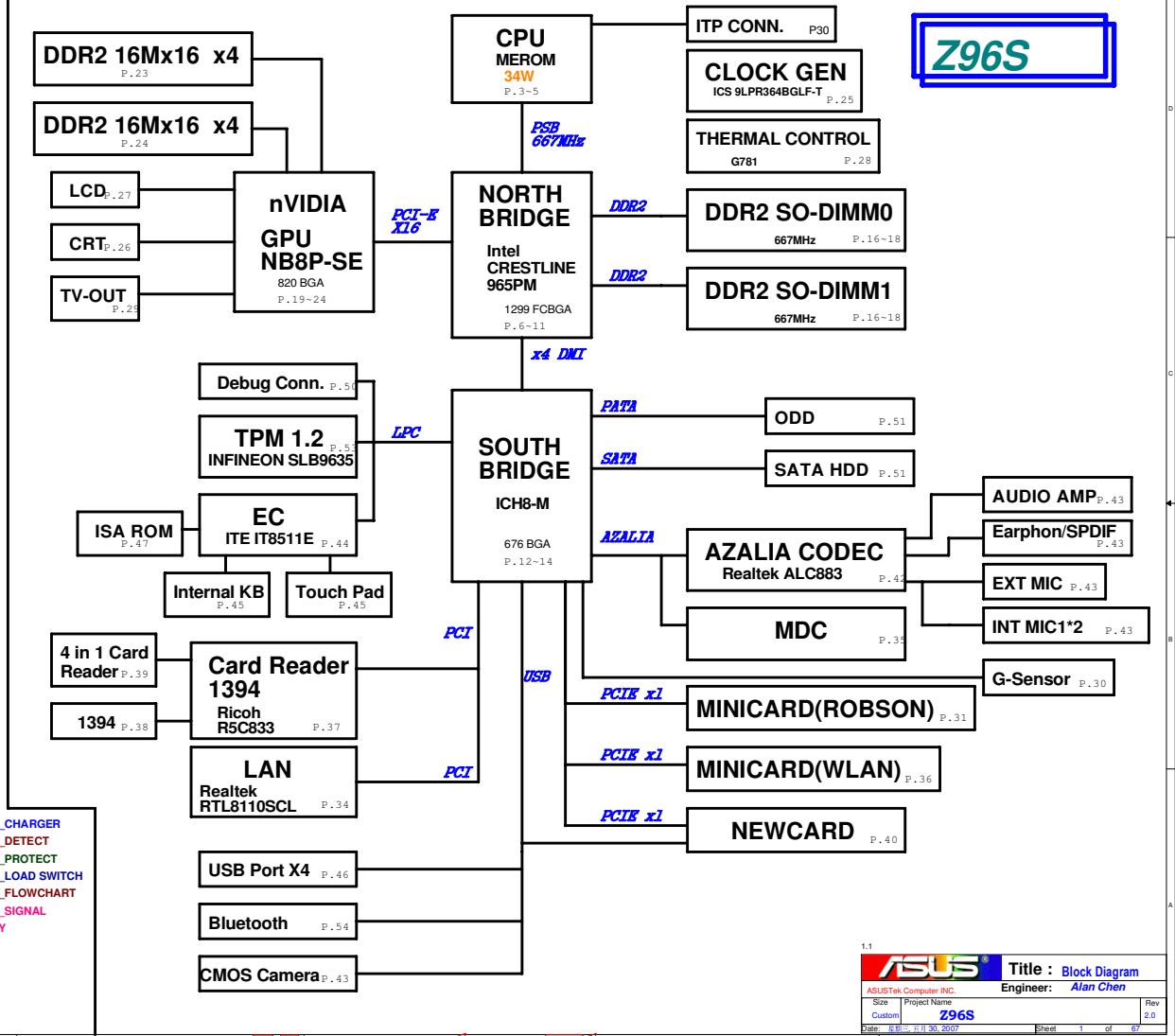



- 01_Block Diagram
- 02_System Setting
- 03_Merom CPU (1)
- 04_Merom CPU (2)
- 05_CPU CAPS.
- 06_965PM-CPU (1)
- 07_965PM-DDR2/PEG (2)
- 08_965PM-DDR2 BUS (3)
- 09_965PM-POWER (4)
- 10_965PM-POWER (5)
- 11_965PM-GND/STRAPPING (6)
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- 22_VGA_nVIDIA_NB8P_PCH-E&PWR(4)
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- 24_VGA_nVIDIA_NB8P_VRAM_B(6)
- 25_CLOCK_GEN-ICS9LPR364AGLF-T
- 26_CRT CONNECTOR
- 27_LVDS & INVERTER CONNECTOR
- 28_THER SENSOR & FAN
- 29_TV OUT CONN
- 30_G-SENSOR & ITP
- 31_MINI CARD -- ROBSON
- 32_SWITCH
- 33_DISCHARGE
- 34_GIGALAN-RTL8110SCL
- 35_MDC&RJ45&RJ11
- 36_MINI CARD -- WLAN
- 37_RICOH-R5C833_PCI
- 38_RICOH-R5C833_1394SD
- 39_4 in 1 CARD READER
- 40_NEWCARD
- 41_Port Bar
- 42_AUDIO-CODEC-ALC882
- 43_AUDIO AMP & JACK
- 44_EC-IT8511E
- 45_Touch Pad/ KB
- 46_USB CONN
- 47_ISA ROM
- 48_LED
- 49_DCIN & BAT CONN
- 50_Debug CONN.
- 51_SATA-HDD & ODD
- 52_SREW HOLE
- 53_TPM CONNECTOR
- 54_BT CONNECTOR
- 55_POWER_VCORE
- 56_POWER_SYSTEM_+3VO & +5VO
- 57_POWER_1.5VS&1.05VS
- 58_POWER_IQ_DDR & VTT
- 59_POWER_+3VAO
- 60_POWER_VGA_CORE
- 61_POWER_CHARGER
- 62_POWER_DETECT
- 63_POWER_PROTECT
- 64_POWER_LOAD SWITCH
- 65_POWER_FLOWCHART
- 66_POWER_SIGNAL
- 67_HISTORY



1.1

		Title : Block Diagram	
ASUSTek Computer INC.		Engineer: Alan Chen	
Size	Project Name		Rev
Custom	Z96S		
Date: 11/11/2007	Sheet 1 of 87		2.0

<< Kennedy_Zhang >>

EC GPIO SETTING

Pin	Pin Name	Signal Name	Type
32	PWM0/GPA0	BL_PWM_DA	O
33	PWM1/GPA1	FAN_PWM	O
36	PWM2/GPA2	CLK_PWRSERVE#	O
37	PWM3/GPA3	NA	
38	PWM4/GPA4	CHG_LED_UP#	O
39	PWM5/GPA5	PWR_LED_UP#	O
40	PWM6/GPA6	NA	
43	PWM7/GPA7	LCD_BACKOFF#	O
153	RXD/GPB0	NUM_LED	O
154	TXD/GPB1	CAP_LED	O
162	GPB2	SCRL_LED	O
163	SMCLK0/GPB3	SMB0_CLK	IO
164	SMDAT0/GPB4	SMB0_DAT	IO
5	GA20/GPB5	A20GATE	O
6	KBRST#/GPB6	RC_IN#	O
165	GPB7	THRO_CPU	O
47	CLKOUT/GPC0	NA	
169	SMCLK1/GPC1	SMB1_CLK	IO
170	SMDAT1/GPC2	SMB1_DAT	IO
171	GPC3	Mail_LED	O
172	TMR0/WUI2/GPC4	AC_OK#	I
175	GPC5	OP_SD#	O
176	TMR11/WUI3/GPC6	BAT_IN_OC#	I
1	CK32KOUT/GPC7	NA	
26	RH#/WUI0/GPD0	SUSB#	I
29	R12#/WUI1/GPD1	SUSC#	I
30	LPCRST#/WUI4/GPD2	PLT_RST#	I
31	ECSC#/GPD3	EXT_SC#	O
41	GPD4	RF_ON_SW#	O
42	INTP/GPD5	NA	
62	TACH0/GPD6	FAN0_TACH	I
63	TACH1/GPD7	NA	
87	ADC4/GPE0	EMAIL_SW#	I
88	ADC5/GPE1	INTERNET#	I
89	ADC6/GPE2	EXPLORE_SW#	I
90	ADC7/GPE3	DISTP_SW#	I
2	PWRSW/GPE4	PWR_SW#	I
44	WUI5/GPE5	NA	
24	LPCPD#/WUI6/GPE6	NA	
25	CLKRUN#/WUI7/GPE7	BL_DA	O
101	GRJ2/DAC2	BATSEL_2P#	O
102	GRJ3/DAC3	P_PMON	I
81	GPK0/ADC0	EXT_SM#	O
22	ECSM#/GPM0	TP_CLK	IO
116	PS2CLK2/GPF4	TP_DAT	IO
117	PS2DAT2/GPF5	NA	
118	PS2CLK3/GPF6	NA	
119	PS2DAT3/GPF7	FA16	O
113	FA16/GPG0	FA17	O
112	FA17/GPG1	FA18	O
104	FA18/GPG2	NA	
103	FA19/GPG3	LID_EC#	I
3	FA20/GPG4	PMTHERM#	O
4	FA21/GPG5	THRM_CPU#	I
27	LPC80HL/GPG6	AC_APR_UC#	I
28	LPC80LL/GPG7		

Pin	Pin Name	Signal Name	Type
48	GPIO0	VSUS_ON	O
54	GPIO1	VSUS_GD#	I
55	GPIO2	CPUPWR_GD#	I
69	GPIO3	PM_PWRBTN#	O
70	GPIO4	SUSC_ON	O
75	GPIO5	SUSB_ON	O
76	GPIO6	CPU_VRON	O
105	GPIO7	PM_RSMRST#	O
148	GPIO8	SB_PWRGD	O
149	GPIO9	NA	
152	GPIO10	MCHOK	I
155	GPIO11	CHG_EN#	O
156	GPIO12	PRECHG	O
168	GPIO13	BAT_LL#	O
174	GPIO14	BAT_LEARN	O

ICH8-M GPIO SETTING

Pin	Pin Name	Signal Name	Type	Power_Well	Default
AG12	GPIO0/BMBUSY#	PM_BMBUSY#	IO	Core(To:3.3V)	GPI
AJ8	GPIO1/TACH1	VDDR_SELO	IO	Core(To:3.3V)	GPI
F8	GPIO2/PIRQE#	INT_SHIFT_LOW#	I(OD)	Core(To:3.3V)	GPI
G11	GPIO3/PIRQF#	INT_SHIFT_HIGH#	I(OD)	Core(To:3.3V)	GPI
F12	GPIO4/PIRQG#	PCL_INTG#	I(OD)	Core(To:3.3V)	GPI
B3	GPIO5/PIROH#	PCL_INTH#	I(OD)	Core(To:3.3V)	GPI
AJ9	GPIO6/TACH2	VDDR_SEL1	IO	Core(To:3.3V)	GPI
AH9	GPIO7/TACH3	VDDR_SEL2	IO	Core(To:3.3V)	GPI
AE16	GPIO8	EXT_SM#	IO	SUS(To:3.3V)	GPI
AG19	GPIO9/WOL_EN	TP	IO	SUS(To:3.3V)	GPI
AJ24	GPIO10/CLGPI01	TP	IO	SUS(To:3.3V)	GPI
AG22	SMBALERT#/GPIO11	NC	IO	SUS(To:3.3V)	Native
AC19	GPIO12	EXT_SC#	IO	SUS(To:3.3V)	GPI
AH21	GPIO13/GLAN_DOCL#	NC	IO	SUS(To:3.3V)	Native
AF22	GPIO14/CLGPI02	TP	IO	SUS(To:3.3V)	GPI
AE20	GPIO15/STP_PCH#	STP_PCH#	IO	SUS(To:3.3V)	Native
AJ14	GPIO16/DPRSLPVR	PM_DPRSLPVR	IO	Core(To:3.3V)	Native
AG8	GPIO17/TACH0	PM_EXTTS#0	IO	Core(To:3.3V)	GPI
AH12	GPIO18	VCORE_SEL0	IO	Core(To:3.3V)	GPO
AJ10	GPIO19/SATA1GP	CB_SD#	IO	Core(To:3.3V)	GPI
AE11	GPIO20	VCORE_SEL1	IO	Core(To:3.3V)	GPO
AJ12	GPIO21/SATA0GP	WLAN_BT_LED_EN#	IO	Core(To:3.3V)	GPI
AG10	GPIO22/SCLOCK	TP	IO	Core(To:3.3V)	GPI
E6	GPIO23/LDRQ1#	TP	IO	Core(To:3.3V)	Native
AJ27	GPIO24/CLGPI00	TP	IO	SUS(To:3.3V)	GPO
AG18	GPIO25/STP_CPU#	STP_CPU#	IO	SUS(To:3.3V)	Native
AH27	GPIO26/S4_STATE#	TP	IO	SUS(To:3.3V)	Native
AH25	GPIO27/ORT_STATE0	VGMCH_SELO	IO	SUS(To:3.3V)	GPO
AD16	GPIO28/ORT_STATE1	VGMCH_SEL1	IO	SUS(To:3.3V)	GPO
AG17	GPIO29/OC#5	USB_OC#5	IO	SUS(To:3.3V)	Native
AD12	GPIO30/OC#6	NEWCARD_OC#	IO	SUS(To:3.3V)	Native
AJ18	GPIO31/OC#7	USB_OC#7	IO	SUS(To:3.3V)	Native
AH11	GPIO32/CLKRUN#	PM_CLKRUN#	IO	Core(To:3.3V)	Native
AE10	GPIO33/HDA_DOCK_EN#	TP	IO	Core(To:3.3V)	GPO
AG14	GPIO34/HDA_DOCK_RST#	TP	IO	Core(To:3.3V)	GPO
AG13	GPIO35/SATACLKREQ#	VGPU_SEL1	IO	Core(To:3.3V)	GPO
AF11	GPIO36/SATA2GP	WLAN_ON#	IO	Core(To:3.3V)	GPI
AG11	GPIO37/SATA3GP	BT_ON#	IO	Core(To:3.3V)	GPI
AF9	GPIO38/SLOAD	PM_EXTTS#1	IO	Core(To:3.3V)	GPI
AJ11	GPIO39/SDATAOUT0	CLK_PWRSERVE#	IO	Core(To:3.3V)	GPI
AG16	GPIO40/OC1#	USB_CON_OC01#	IO	SUS(To:3.3V)	Native
AG15	GPIO41/OC2#	USB_CON_OC23#	IO	SUS(To:3.3V)	Native

PCI Device	IDSEL#	REQ/GNT#	Interrupts
CARD READER	AD17	REQ#0/GNT#0	INTB-->INTB
1394	AD17	REQ#0/GNT#0	INTA-->INTA
LAN	AD23	REQ#2/GNT#2	INTA-->INTC

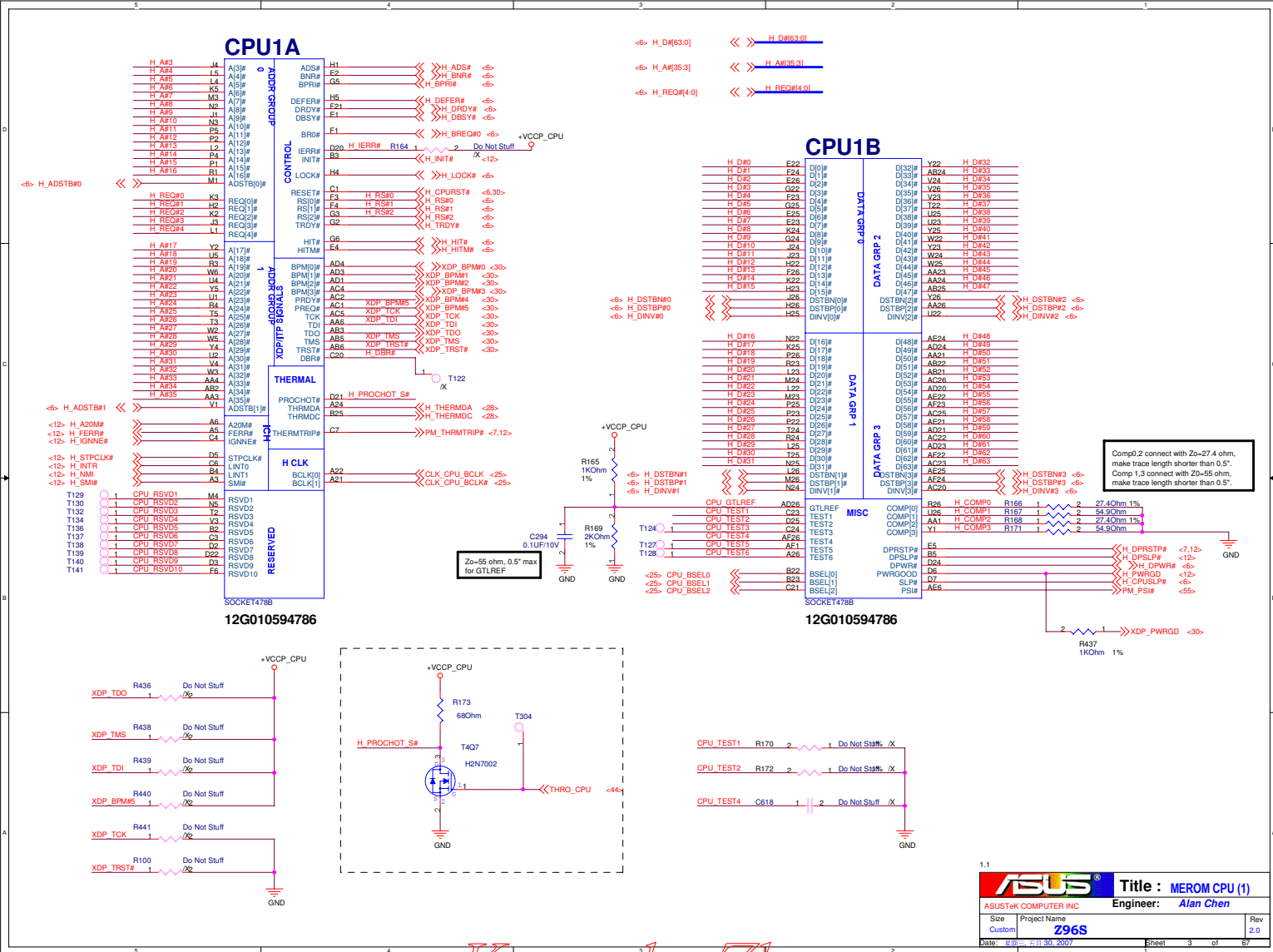
SM-Bus Device	SM-Bus Address
Clock Generator	1101001x (D2)
SO-DIMM 0	1010000x (A0)
SO-DIMM 1	1010001x (A2)
Thermal Sensor	0101110x (5C)

Pin	Pin Name	Signal Name	Type	Power_Well	Default
AD16	GPIO42/OC3#	USB_CON_OC23#	IO	SUS(To:3.3V)	Native
AG17	GPIO43/OC4#	USB_CON_OC4#	IO	SUS(To:3.3V)	Native
NA	GPIO44	NA	IO	NA	NA
NA	GPIO45	NA	IO	NA	NA
NA	GPIO46	NA	IO	NA	NA
NA	GPIO47	NA	IO	NA	NA
AD10	GPIO48/SDATAOUT1	TP	IO	Core(To:3.3V)	GPI
AG29	GPIO49/CPUPWRGD	H_PWRGD	IO	V_CPU_IO	Native
E18	GPIO50/REQ1#	PCL_REQ#1	IO	Core(To:3.5V)	Native
C18	GPIO51/GNT1#	TP	IO	Core(To:3.3V)	Native
B19	GPIO52/REQ2#	PCL_REQ#2	IO	Core(To:3.5V)	Native
F18	GPIO53/GNT2#	PCL_GNT#2	IO	Core(To:3.3V)	Native
A11	GPIO54/REQ3#	PCL_REQ#3	IO	Core(To:3.5V)	Native
C10	GPIO55/GNT3#	NC	IO	Core(To:3.3V)	Native

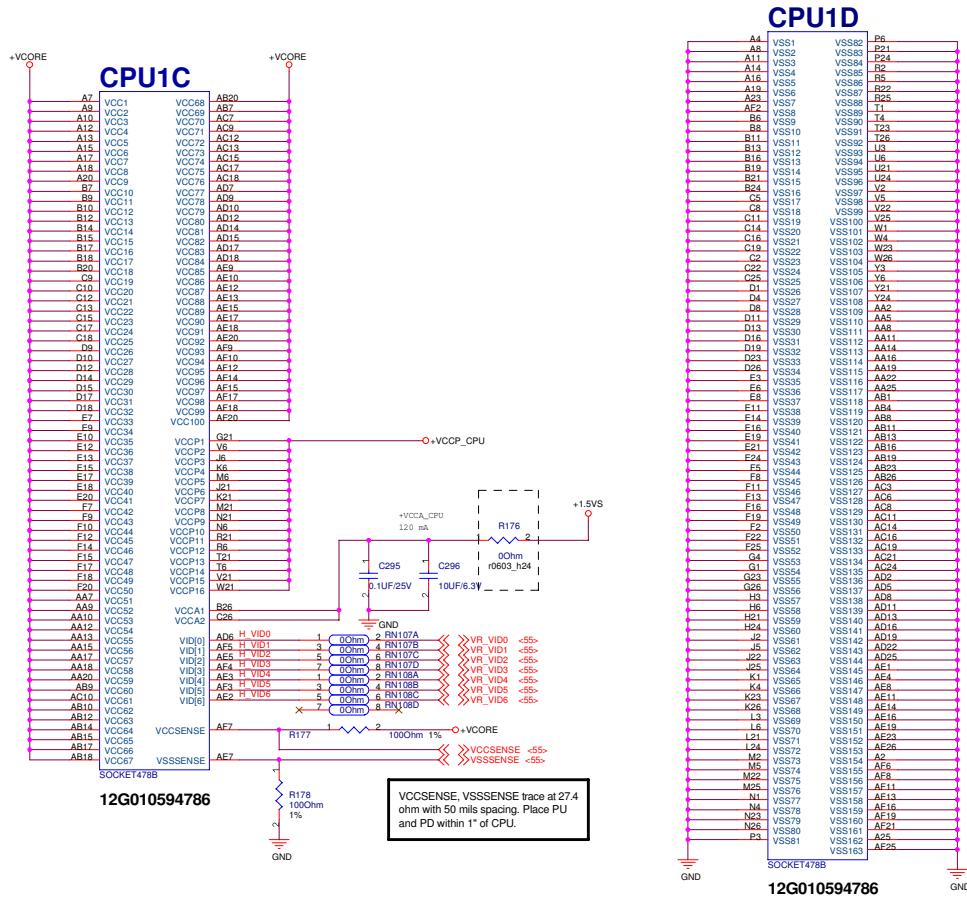
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ASUS		Title : System Setting	
ASUSTek Computer INC.		Engineer: Alan Chen	
Size	Project Name		Rev
Custom	Z96S		2.0
Date: 10/10/2007		Sheet	2 of 67

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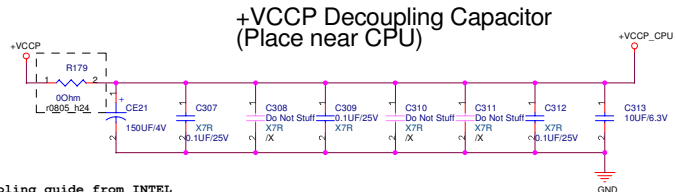
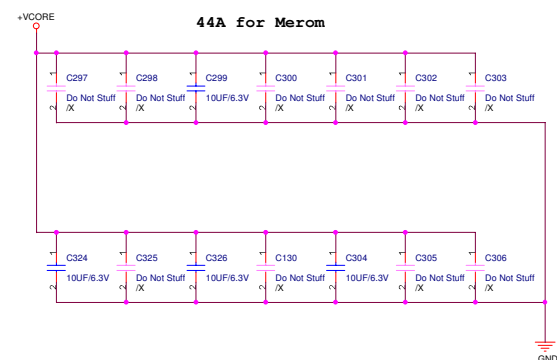
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1.1

ASUS		Title : MEROM CPU (2)	
ASUSTeK COMPUTER INC.		Engineer: Alan Chen	
Size	Project Name	Rev	
Custom	Z96S	2.0	
Date: 08-11-30-2007	Sheet 4 of 87		

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Decoupling guide from INTEL

VCCORE	22uF/10V	* 32pcs
	330uF/2V	* 6pcs
VCCP	0.1uF	* 6pcs for CPU
	150uF	* 1pcs for CPU

1.1

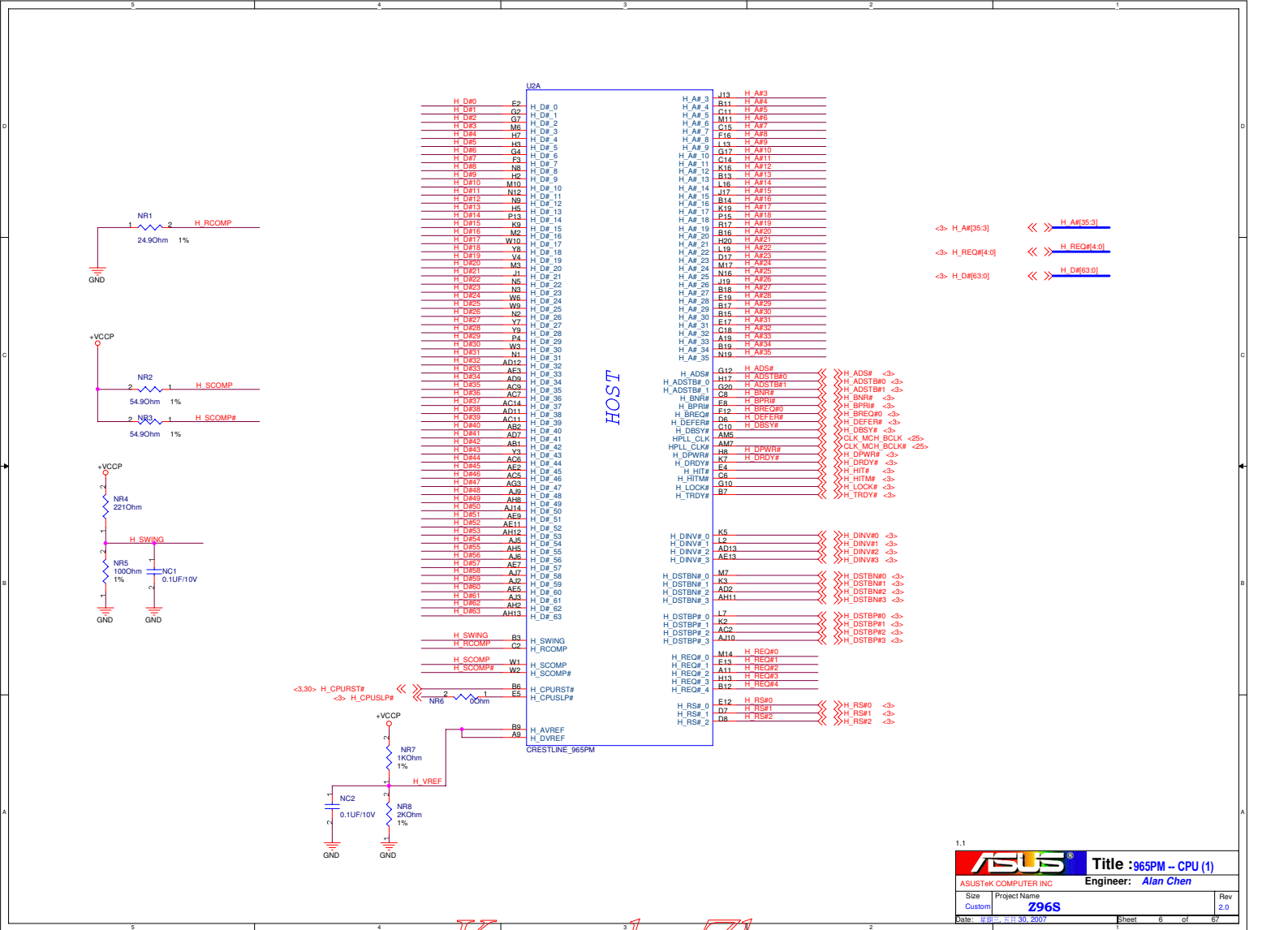
ASUS Title :CPU CAP and HOLES

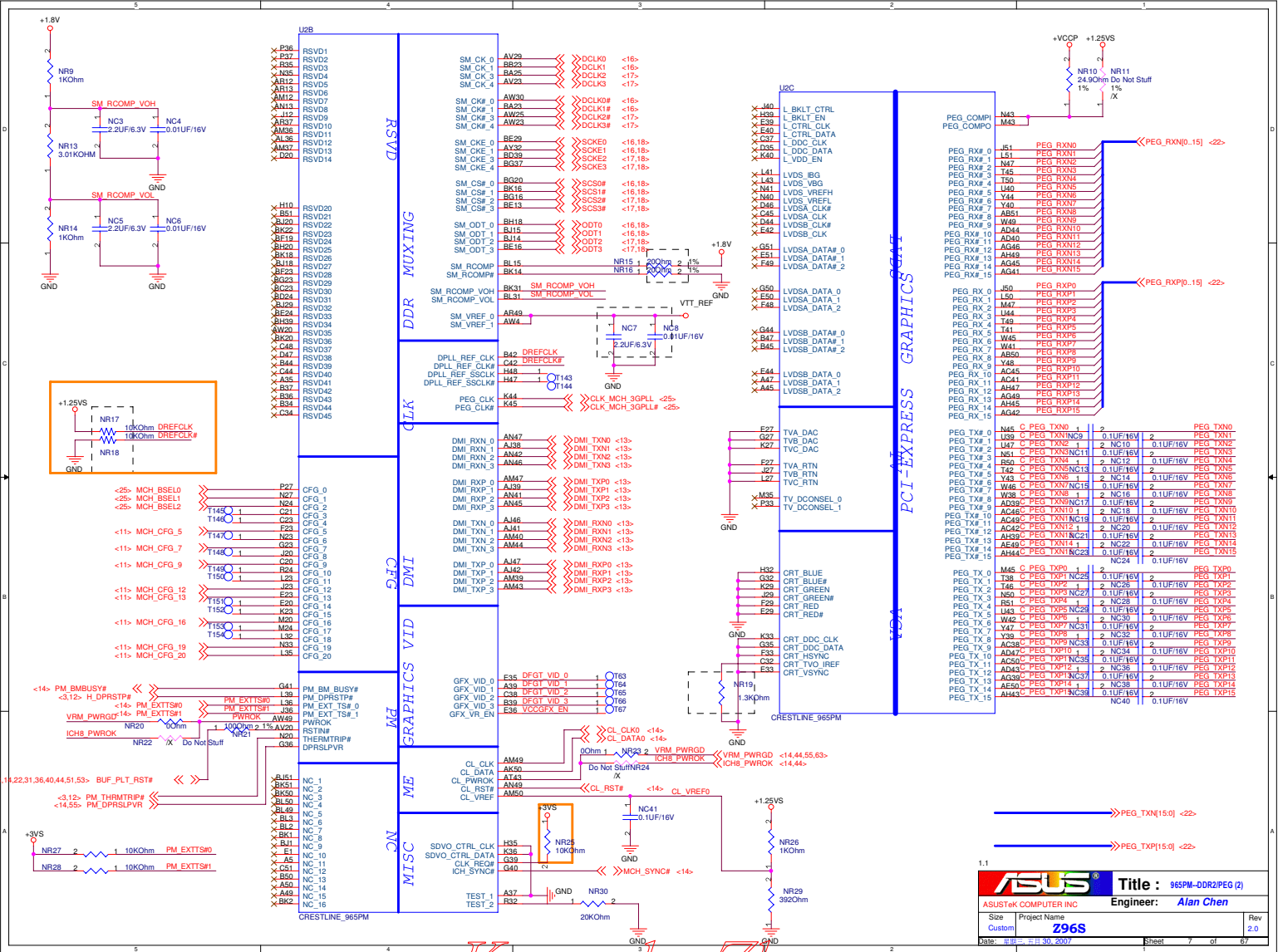
ASUSTek COMPUTER INC. NBI Engineer: Alan Chen

Size	Project Name	Rev
Custom	Z96S	2.0

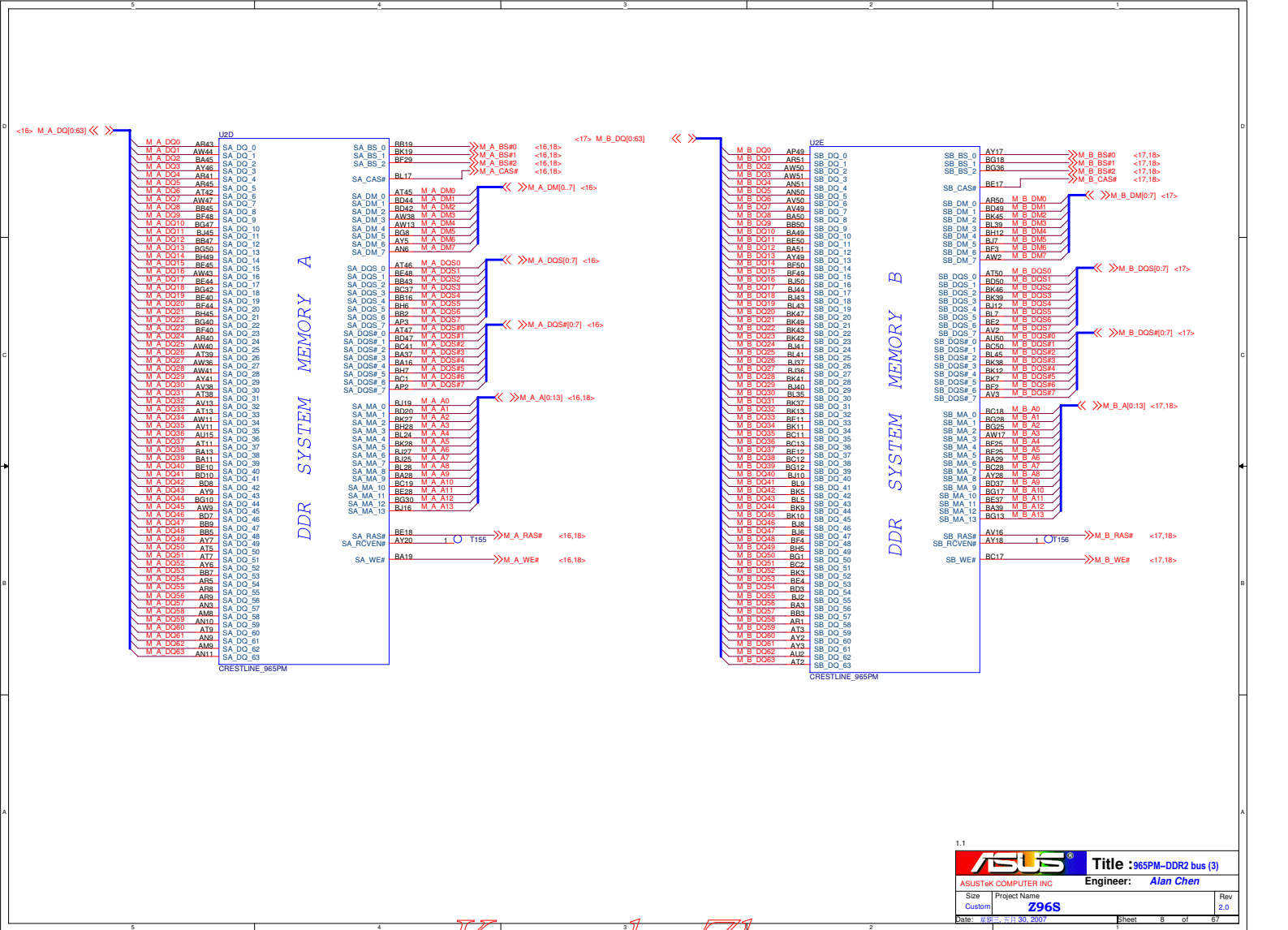
Date: 2007-11-30 Sheet 5 of 67

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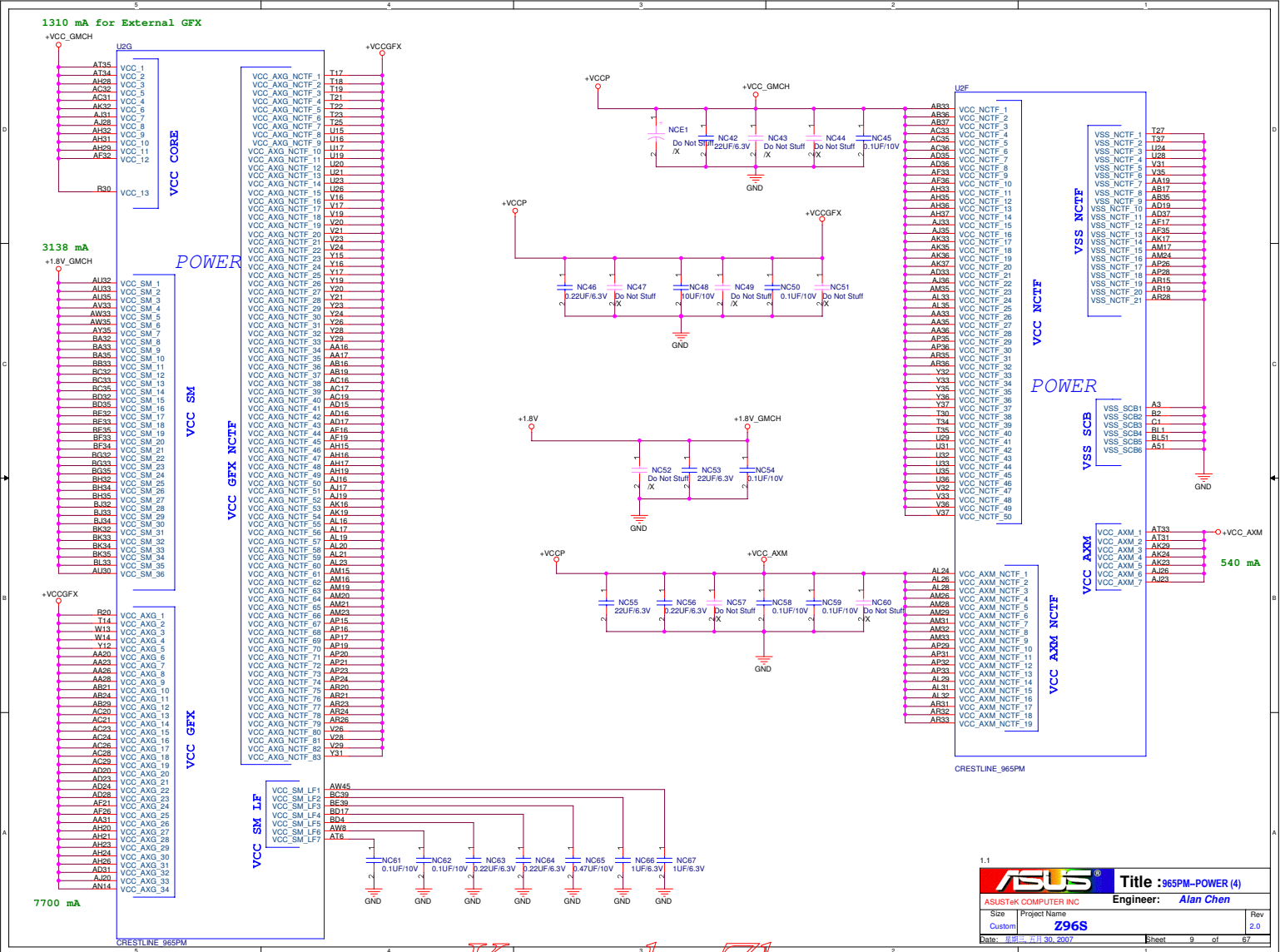


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1.1		ASUS®		Title : 965PM-DDR2 bus (3)	
ASUSTeK COMPUTER INC.		Engineer: Alan Chen			
Size	Project Name			Rev	
Custom	Z96S			2.0	
Date: 07/11/2007				Sheet	8 of 87

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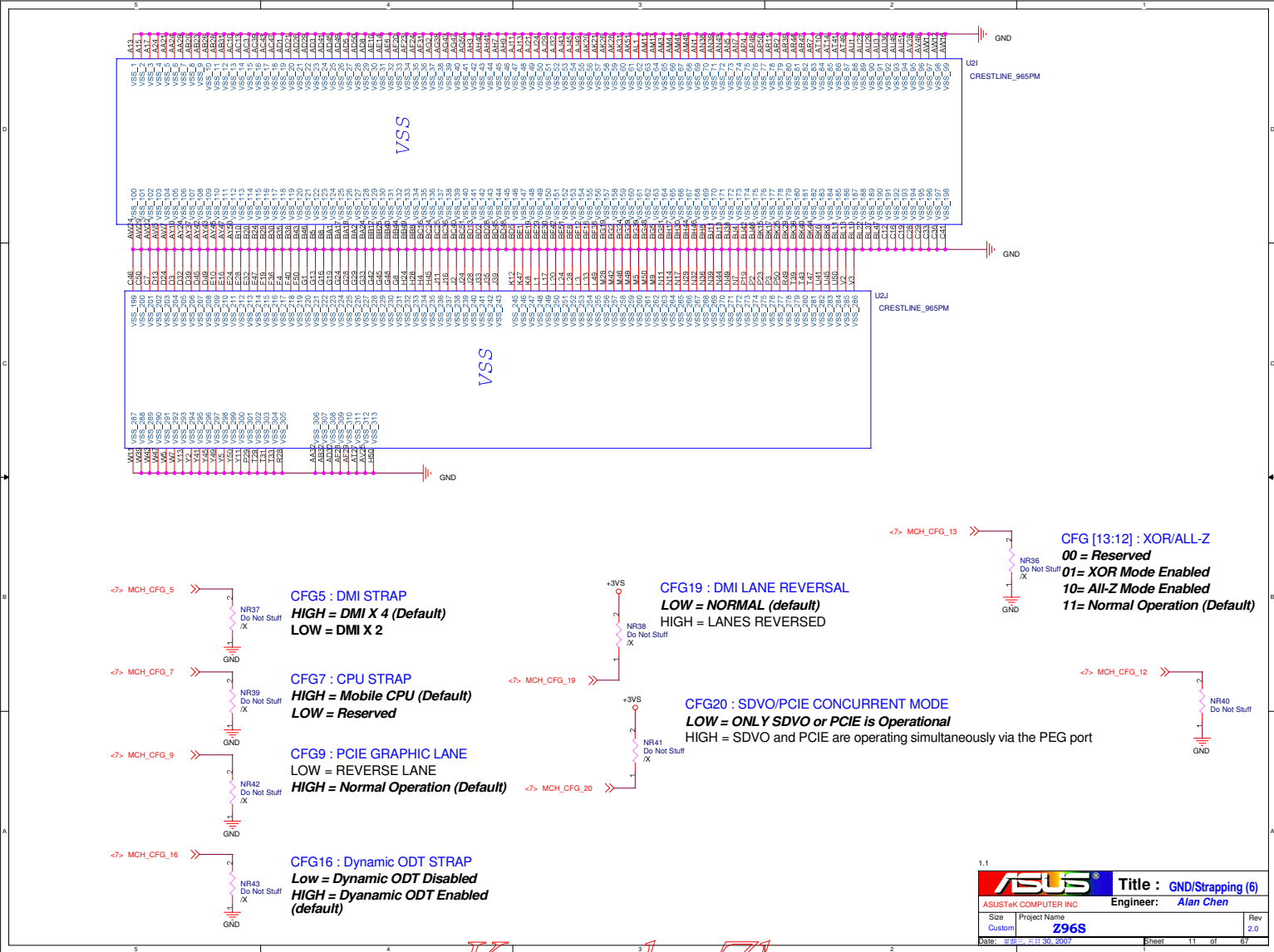


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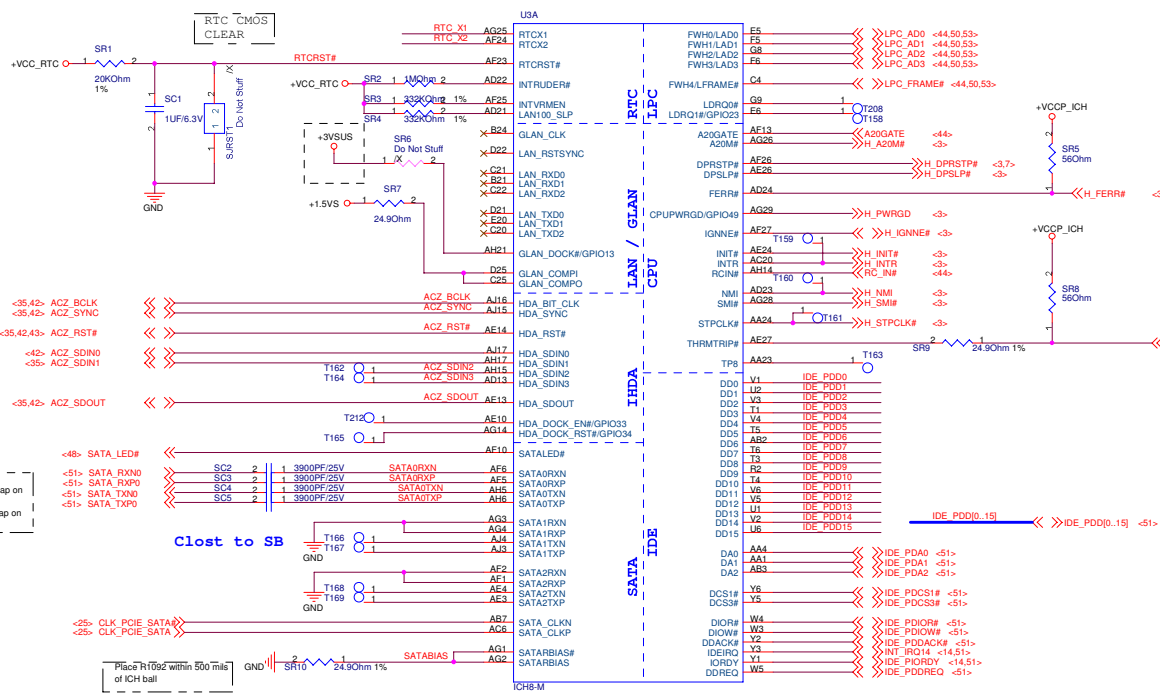
The schematic diagram illustrates the power and signal architecture of the 965M-POWER (5) circuit. It features a central 'POWER' block and a 'CRESTLINE_965PM' block. The circuit is divided into several functional sections:

- CRT:** Includes components like J32, J33, J34, J35, J36, J37, J38, J39, J40, J41, J42, J43, J44, J45, J46, J47, J48, J49, J50, J51, J52, J53, J54, J55, J56, J57, J58, J59, J60, J61, J62, J63, J64, J65, J66, J67, J68, J69, J70, J71, J72, J73, J74, J75, J76, J77, J78, J79, J80, J81, J82, J83, J84, J85, J86, J87, J88, J89, J90, J91, J92, J93, J94, J95, J96, J97, J98, J99, J100, J101, J102, J103, J104, J105, J106, J107, J108, J109, J110, J111, J112, J113, J114, J115, J116, J117, J118, J119, J120, J121, J122, J123, J124, J125, J126, J127, J128, J129, J130, J131, J132, J133, J134, J135, J136, J137, J138, J139, J140, J141, J142, J143, J144, J145, J146, J147, J148, J149, J150, J151, J152, J153, J154, J155, J156, J157, J158, J159, J160, J161, J162, J163, J164, J165, J166, J167, J168, J169, J170, J171, J172, J173, J174, J175, J176, J177, J178, J179, J180, J181, J182, J183, J184, J185, J186, J187, J188, J189, J190, J191, J192, J193, J194, J195, J196, J197, J198, J199, J200, J201, J202, J203, J204, J205, J206, J207, J208, J209, J210, J211, J212, J213, J214, J215, J216, J217, J218, J219, J220, J221, J222, J223, J224, J225, J226, J227, J228, J229, J230, J231, J232, J233, J234, J235, J236, J237, J238, J239, J240, J241, J242, J243, J244, J245, J246, J247, J248, J249, J250, J251, J252, J253, J254, J255, J256, J257, J258, J259, J260, J261, J262, J263, J264, J265, J266, J267, J268, J269, J270, J271, J272, J273, J274, J275, J276, J277, J278, J279, J280, J281, J282, J283, J284, J285, J286, J287, J288, J289, J290, J291, J292, J293, J294, J295, J296, J297, J298, J299, J300, J301, J302, J303, J304, J305, J306, J307, J308, J309, J310, J311, J312, J313, J314, J315, J316, J317, J318, J319, J320, J321, J322, J323, J324, J325, J326, J327, J328, J329, J330, J331, J332, J333, J334, J335, J336, J337, J338, J339, J340, J341, J342, J343, J344, J345, J346, J347, J348, J349, J350, J351, J352, J353, J354, J355, J356, J357, J358, J359, J360, J361, J362, J363, J364, J365, J366, J367, J368, J369, J370, J371, J372, J373, J374, J375, J376, J377, J378, J379, J380, J381, J382, J383, J384, J385, J386, J387, J388, J389, J390, J391, J392, J393, J394, J395, J396, J397, J398, J399, J400, J401, J402, J403, J404, J405, J406, J407, J408, J409, J410, J411, J412, J413, J414, J415, J416, J417, J418, J419, J420, J421, J422, J423, J424, J425, J426, J427, J428, J429, J430, J431, J432, J433, J434, J435, J436, J437, J438, J439, J440, J441, J442, J443, J444, J445, J446, J447, J448, J449, J450, J451, J452, J453, J454, J455, J456, J457, J458, J459, J460, J461, J462, J463, J464, J465, J466, J467, J468, J469, J470, J471, J472, J473, J474, J475, J476, J477, J478, J479, J480, J481, J482, J483, J484, J485, J486, J487, J488, J489, J490, J491, J492, J493, J494, J495, J496, J497, J498, J499, J500, J501, J502, J503, J504, J505, J506, J507, J508, J509, J510, J511, J512, J513, J514, J515, J516, J517, J518, J519, J520, J521, J522, J523, J524, J525, J526, J527, J528, J529, J530, J531, J532, J533, J534, J535, J536, J537, J538, J539, J540, J541, J542, J543, J544, J545, J546, J547, J548, J549, J550, J551, J552, J553, J554, J555, J556, J557, J558, J559, J560, J561, J562, J563, J564, J565, J566, J567, J568, J569, J570, J571, J572, J573, J574, J575, J576, J577, J578, J579, J580, J581, J582, J583, J584, J585, J586, J587, J588, J589, J590, J591, J592, J593, J594, J595, J596, J597, J598, J599, J600, J601, J602, J603, J604, J605, J606, J607, J608, J609, J610, J611, J612, J613, J614, J615, J616, J617, J618, J619, J620, J621, J622, J623, J624, J625, J626, J627, J628, J629, J630, J631, J632, J633, J634, J635, J636, J637, J638, J639, J640, J641, J642, J643, J644, J645, J646, J647, J648, J649, J650, J651, J652, J653, J654, J655, J656, J657, J658, J659, J660, J661, J662, J663, J664, J665, J666, J667, J668, J669, J670, J671, J672, J673, J674, J675, J676, J677, J678, J679, J680, J681, J682, J683, J684, J685, J686, J687, J688, J689, J690, J691, J692, J693, J694, J695, J696, J697, J698, J699, J700, J701, J702, J703, J704, J705, J706, J707, J708, J709, J710, J711, J712, J713, J714, J715, J716, J717, J718, J719, J720, J721, J722, J723, J724, J725, J726, J727, J728, J729, J730, J731, J732, J733, J734, J735, J736, J737, J738, J739, J740, J741, J742, J743, J744, J745, J746, J747, J748, J749, J750, J751, J752, J753, J754, J755, J756, J757, J758, J759, J760, J761, J762, J763, J764, J765, J766, J767, J768, J769, J770, J771, J772, J773, J774, J775, J776, J777, J778, J779, J780, J781, J782, J783, J784, J785, J786, J787, J788, J789, J790, J791, J792, J793, J794, J795, J796, J797, J798, J799, J800, J801, J802, J803, J804, J805, J806, J807, J808, J809, J810, J811, J812, J813, J814, J815, J816, J817, J818, J819, J820, J821, J822, J823, J824, J825, J826, J827, J828, J829, J830, J831, J

<< Kennedy_Zhang HIGH - LANES REVERSED >>



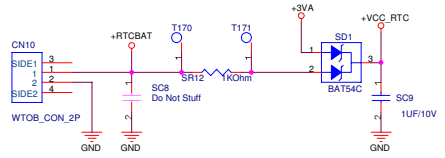
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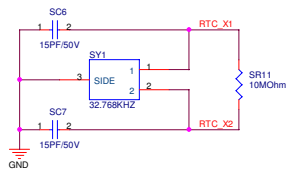
SATA
Distance between the ICH7 and cap on the "P" signal should be identical distance between the ICH7 and cap on the "N" signal for same pair.

SATA if it non-used,
1) SATA[0:3]RXpn SATABIAS, SATABIAS# and SATA_CLKpn should be PD.
2) SATA[0:3]TXpn and SATALED# NO connect.

RTC BAT

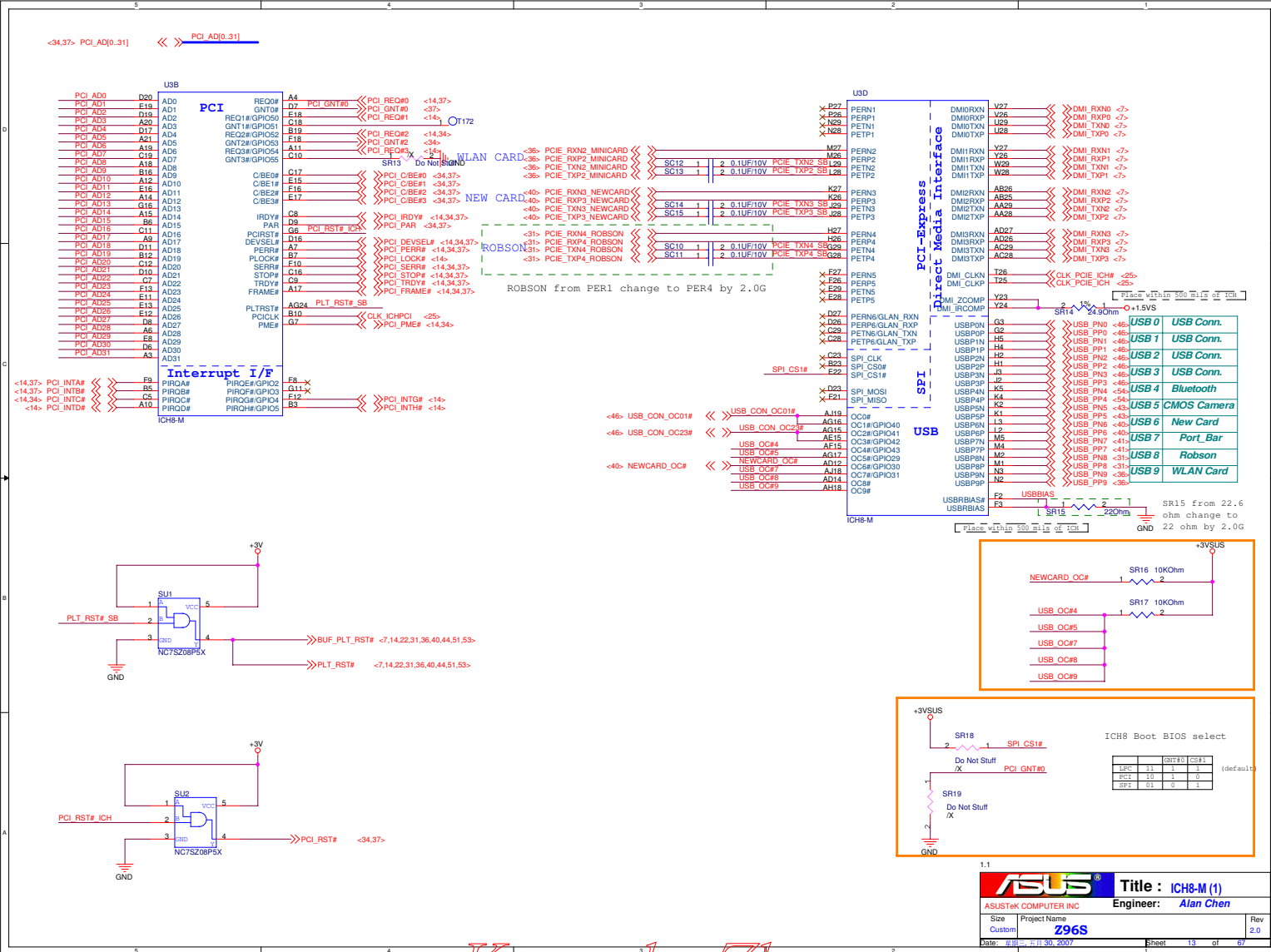


RTC Battery
P/N=07-016322032

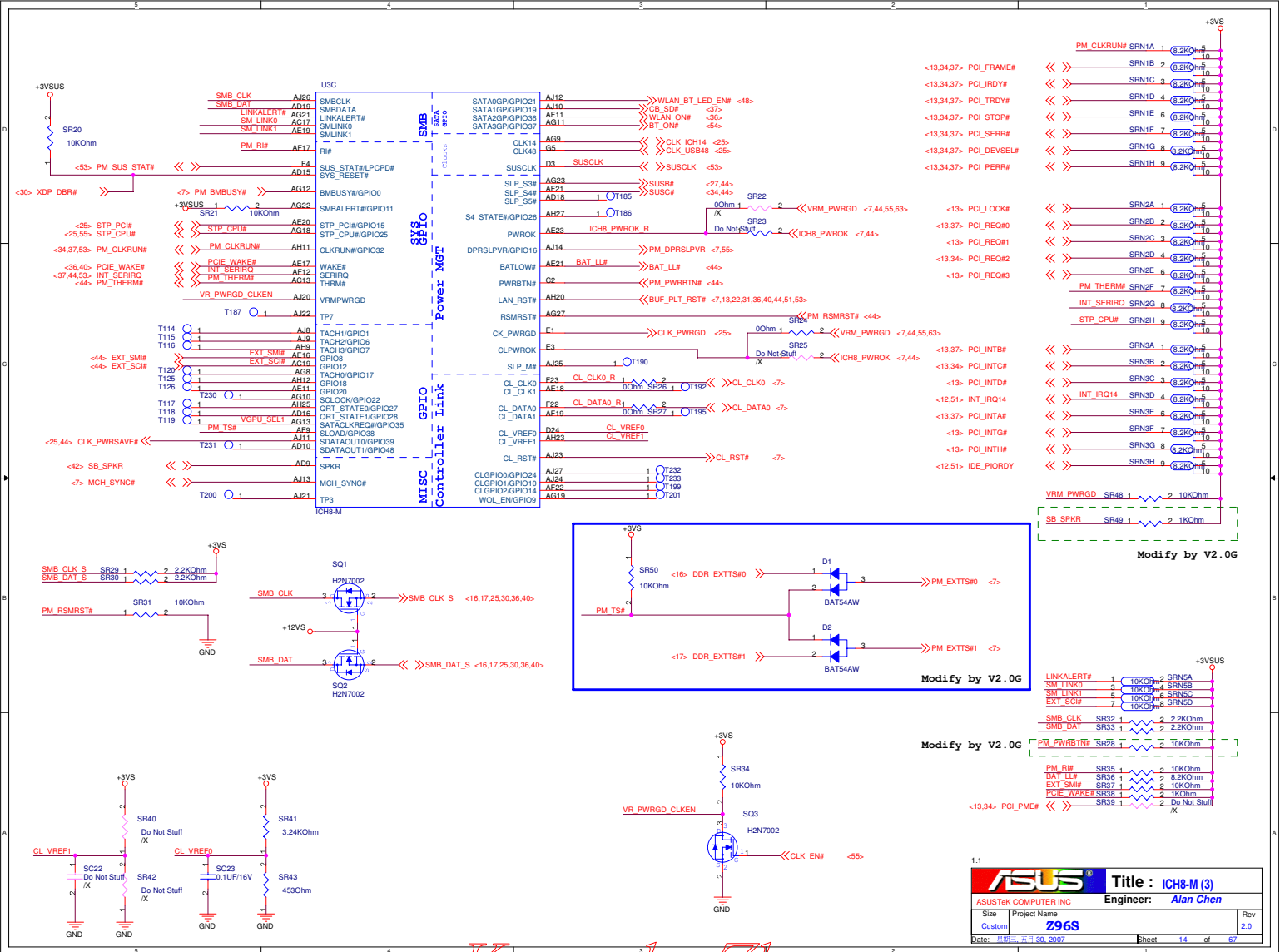


ASUS		Title : ICH8-M (1)	
ASUSTek COMPUTER INC		Engineer: Alan Chen	
Size	Project Name		Rev
Custom	Z96S		2.0
Date: 2007.07.30	Sheet 12	of 67	

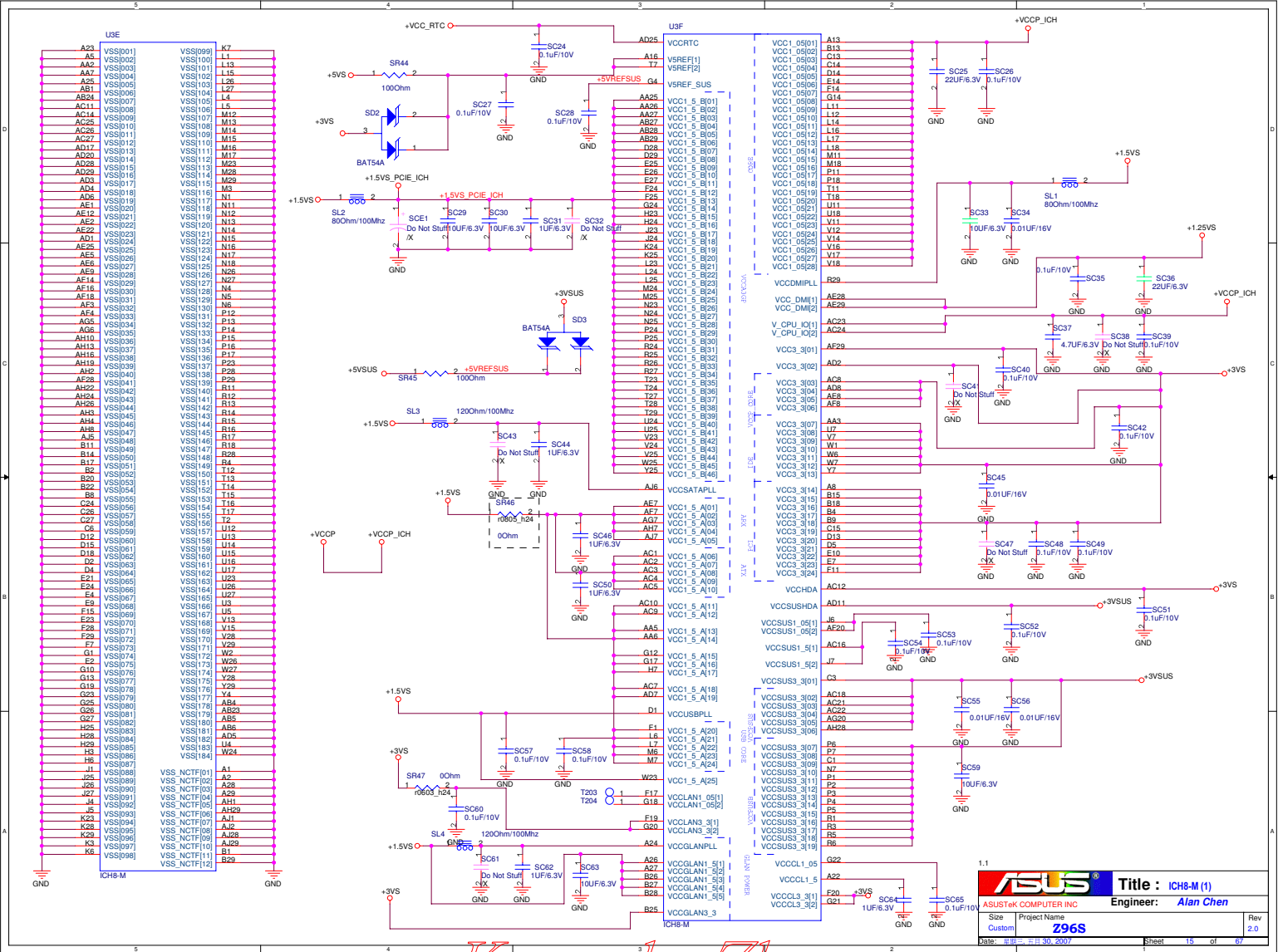
<< Kennedy_Zhang >>



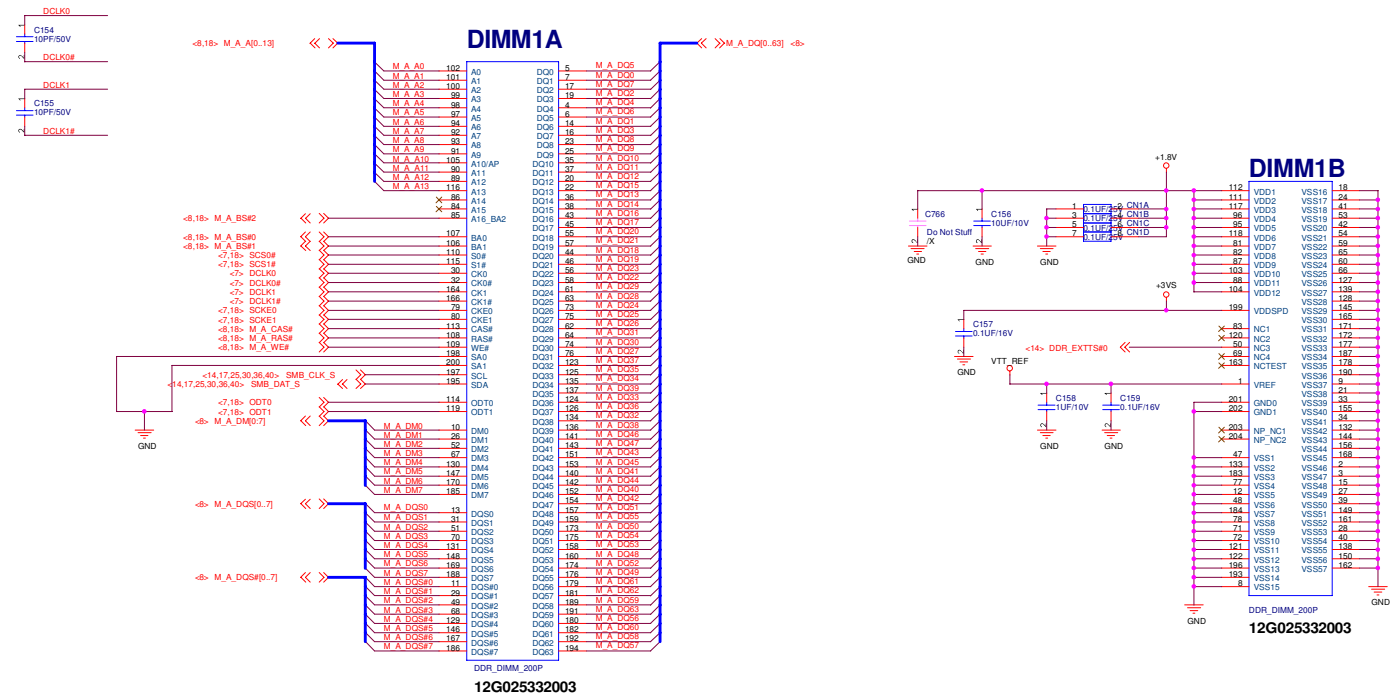
<< Kennedy_Zhang >>



<< Kennedy_Zhang >>



REV Type



1.1

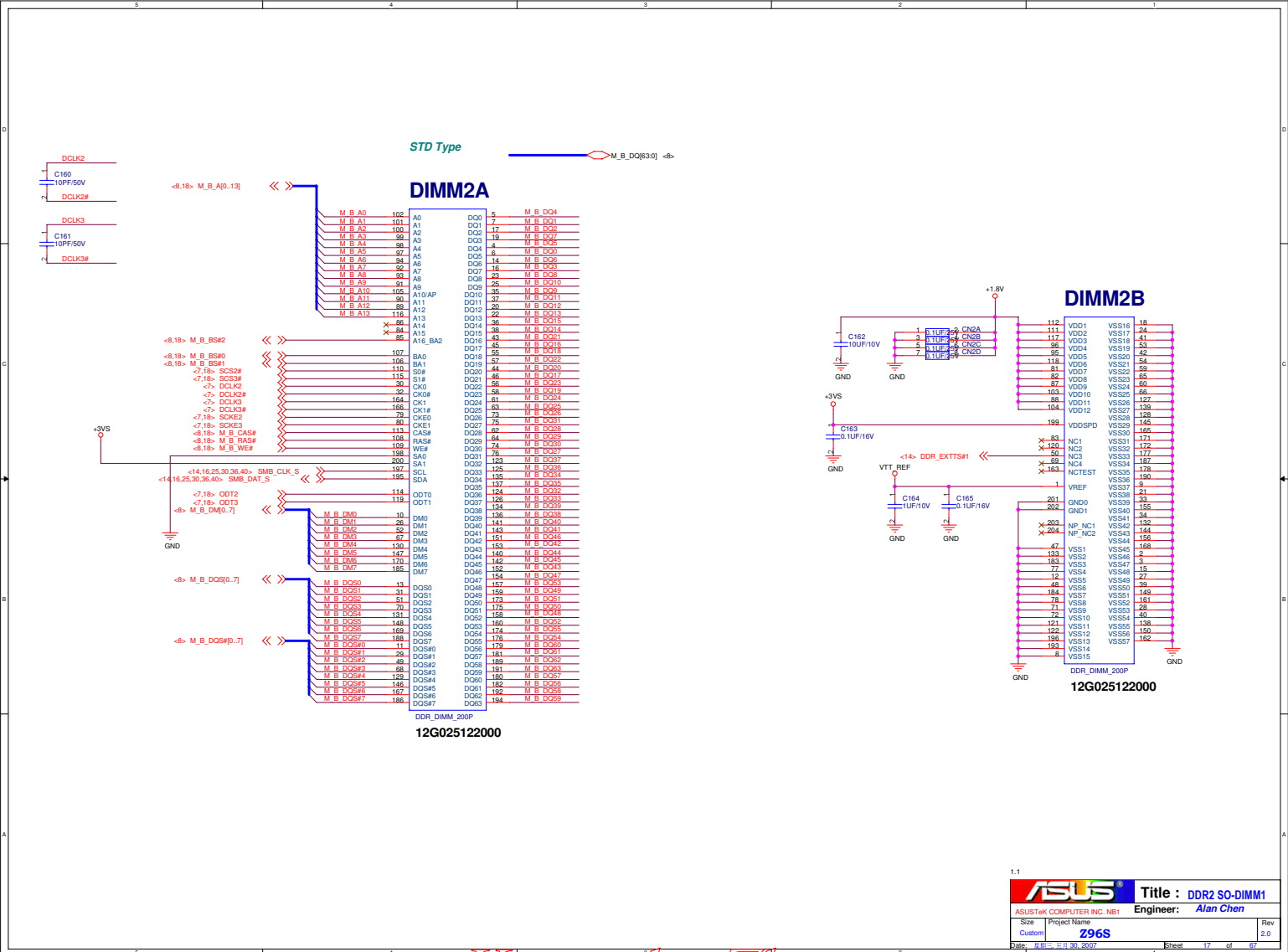


Title : DDR2 SO-DIMM0

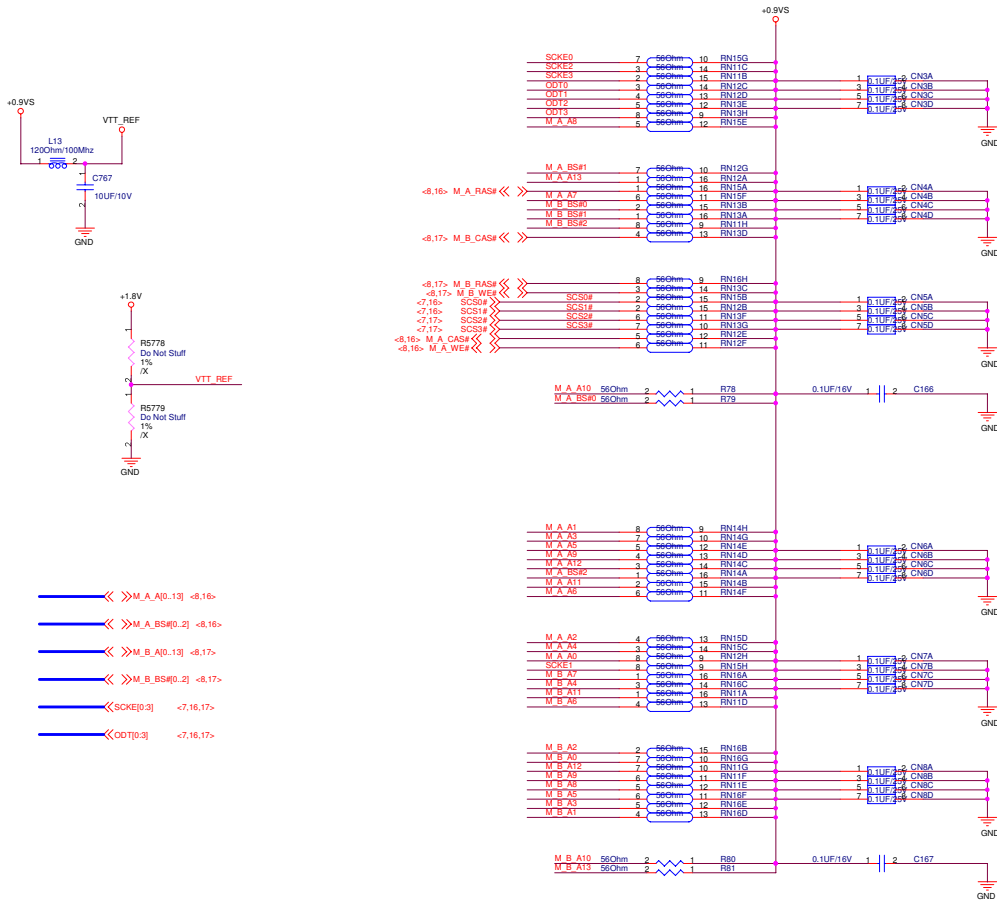
Engineer: *Alan Chen*

Size Custom	Project Name Z96S	Rev 2.0
Date: 星期二, 五月 30, 2007		Sheet 16 of 67

<< Kennedy_Zhang >>



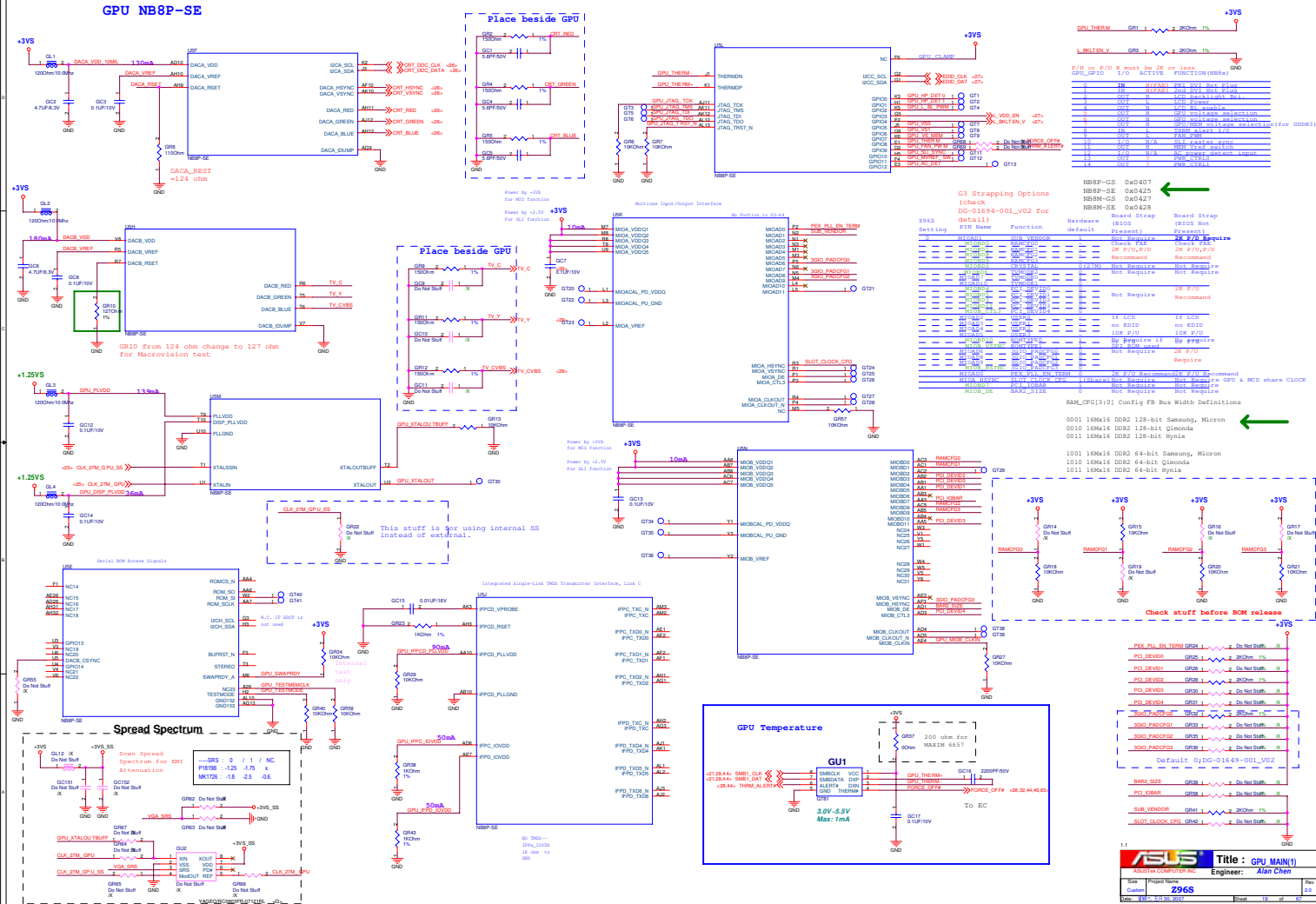
<< Kennedy_Zhang >>



<< M_A_A0[0..13] <8.16>
 << M_B_BS#0[0..2] <8.16>
 << M_B_BS#1[0..2] <8.17>
 << M_B_BS#2[0..2] <8.17>
 << SCKE0[0..3] <7.16,17>
 << ODT0[0..3] <7.16,17>

<< Kennedy_Zhang >>

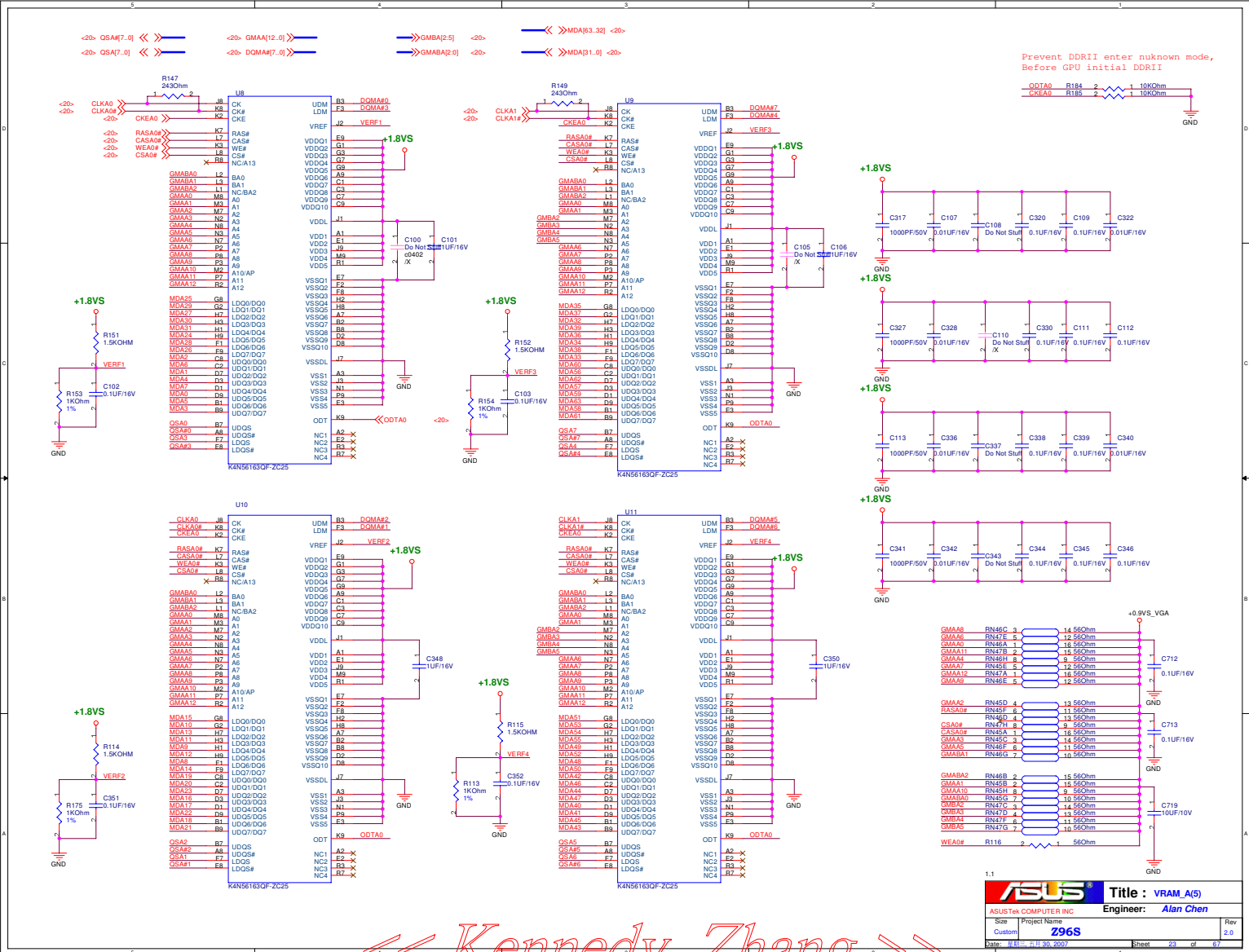
GPU NB8P-SE



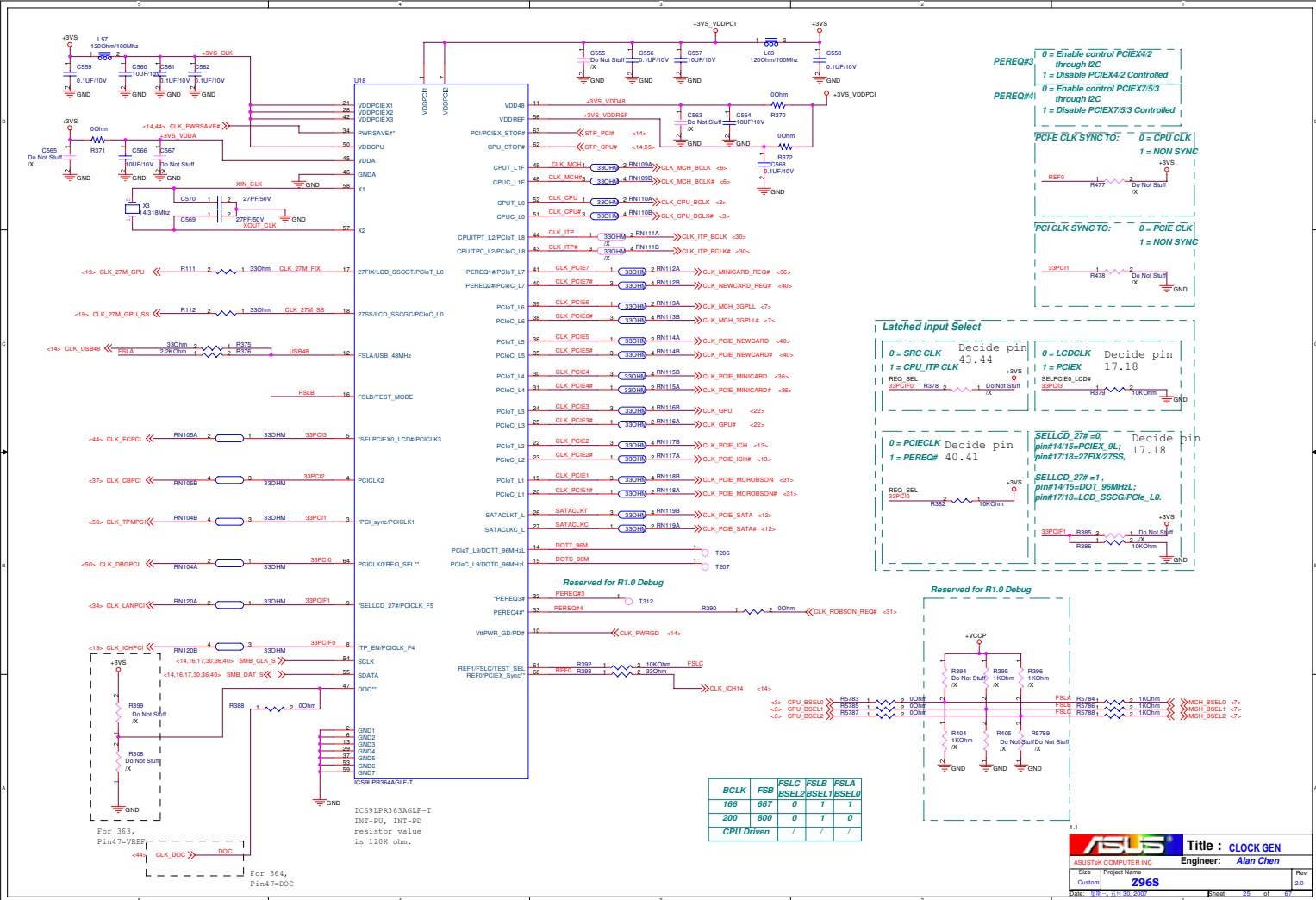
<< Kennedy_Zhang >>



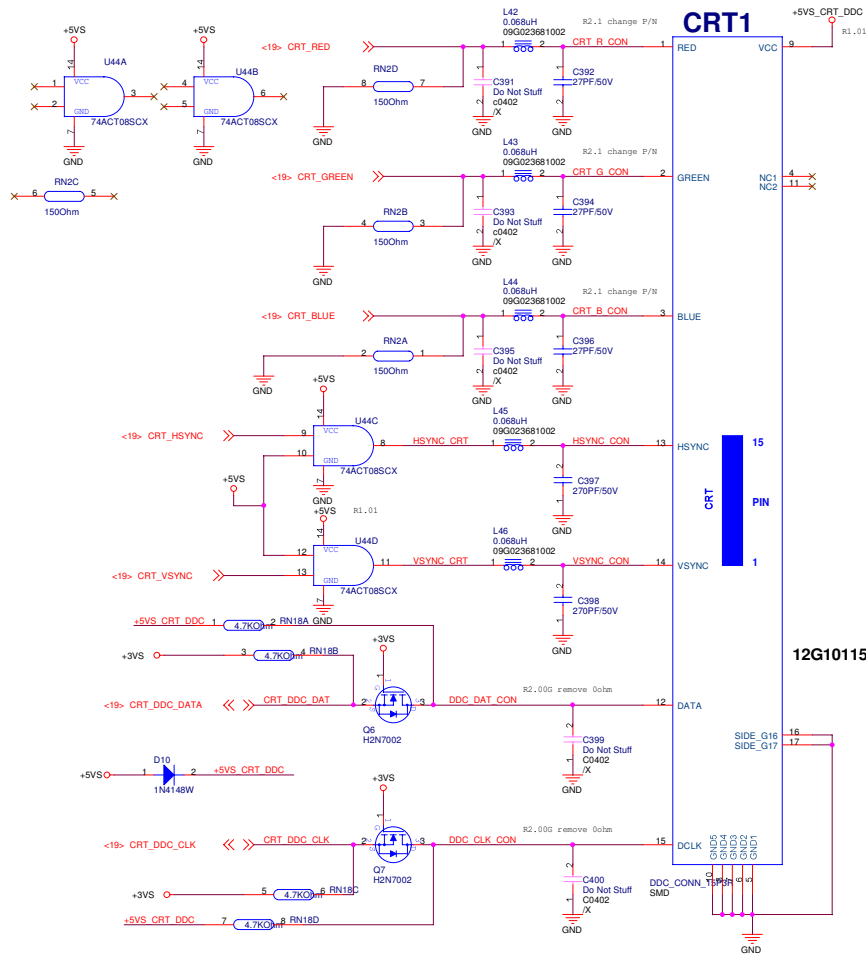
<< Kennedy_Zhang >>



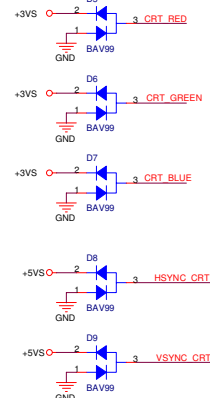




<< Kennedy_Zhang >>



<< CRT_R_CON >> CRT_R_CON <<4>
 << CRT_G_CON >> CRT_G_CON <<4>
 << CRT_B_CON >> CRT_B_CON <<4>
 << DDC_DAT_CON >> DDC_DAT_CON <<4>
 << DDC_CLK_CON >> DDC_CLK_CON <<4>
 << HSYNC_CON >> HSYNC_CON <<4>
 << VSYNC_CON >> VSYNC_CON <<4>



PLACE ESD Diodes near VGA port

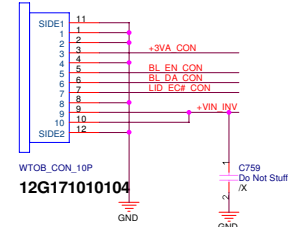
12G10115215B

ASUS		Title : CRT	
ASUSTeK COMPUTER INC		Engineer: Alan Chen	
Size	Project Name		Rev
Custom	Z96S		2.0
Date: 2007.11.30	Sheet 26	of 67	

<< Kennedy_Zhang >>

LCD LVDS Interface

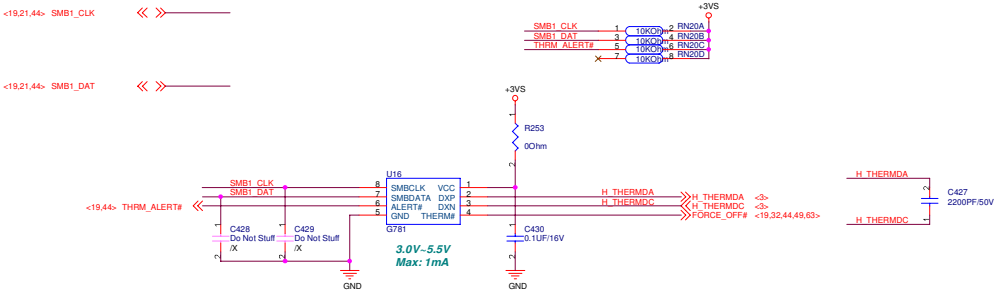
Cable Requirement:
Impedance: 100 ohm +/- 10%
Length Mismatch <= 10 mils
Twisted Pair(Not Ribbon)
Maximum Length <= 16"

[illegible][illegible]

		Title : LVDS & INVERTER	
ASUSTek COMPUTER INC		Engineer: Alan Chen	
Size Custom	Project Name Z96S	Rev 2.0	
Date: 2012.07.26 09:07	Sheet 33 of 53		

<< Kennedy_Zhang >>

Thermal Sensor



Route H_THERMDA and H_THERMDC on the same layer

=====OTHER SIGNALS=====

15 mils

=====GND=====

10 mils

=====H_THERMDA(10 mils)=====

10 mils

=====H_THERMDC(10 mils)=====

10 mils

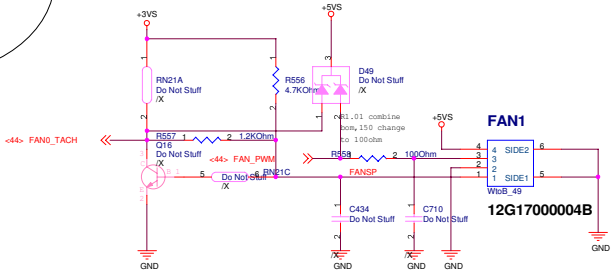
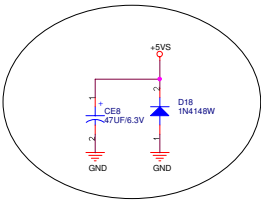
=====GND=====

15 mils

=====OTHER SIGNALS=====

Avoid FSB,Power

DC FAN Control

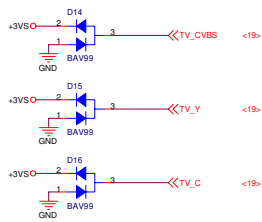


CPU FAN will be forced on:
1) Thermal Sensor Over-temperature
2) WATCHDOG asserted by EC

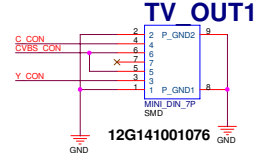
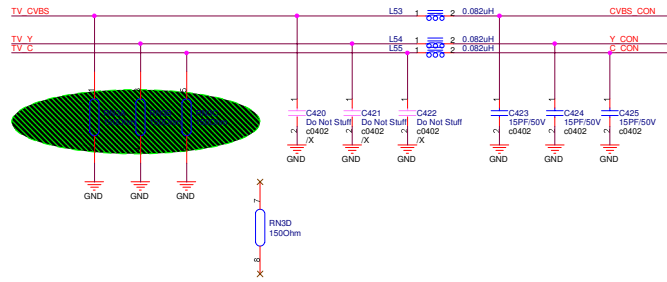
ASUS		Title : THER SENSOR & FAN	
ASUSTek COMPUTER INC.		Engineer: Alan Chen	
Size	Project Name		Rev
Custom	Z96S		2.0
Date: 11/13/2007		Sheet 28 of 87	

<< Kennedy_Zhang >>

TV OUT



PLACE ESD
Diodes near
TV port



ASUS		Title : TV OUT & DVI CON.	
ASUSTek COMPUTER INC.		Engineer: Alan Chen	
Size	Project Name		Rev
Custom	Z96S		2.0
Date: 11/11/2007		Sheet 29 of 87	

<< Kennedy_Zhang >>

5

4

3

2

1

D

D

C

C

B

B

A

A

5

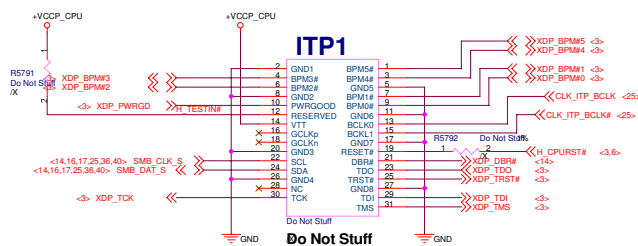
4

3

2

1

ITP



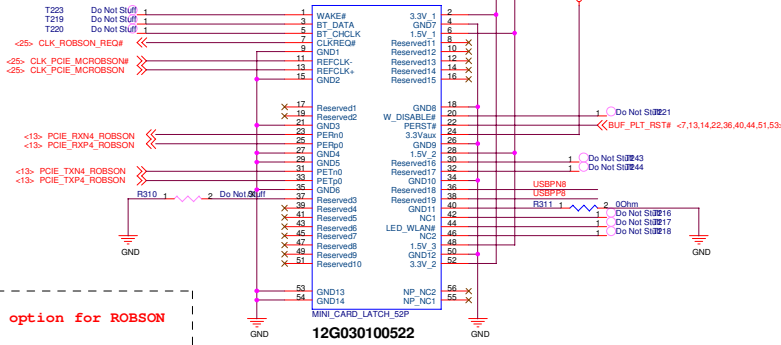
1.1

ASUS		Title : ITP	
ASUSTek Computer INC.		Engineer: Alan Chen	
Size	Project Name	Rev	
Custom	Z96S	2.0	
Date: 11/11/2011	Sheet	36	of 67

<< Kennedy_Zhang >>

ROBSON

ROBSON1



12G030100522

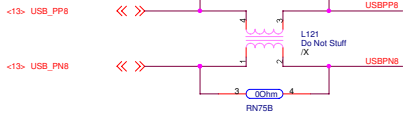
H = 4.0mm

+3.003V~+3.597V
Max= 750 mA

+1.425V~+1.575V
Max= 375 mA

+3.003V~+3.597V
Max= 250 mA

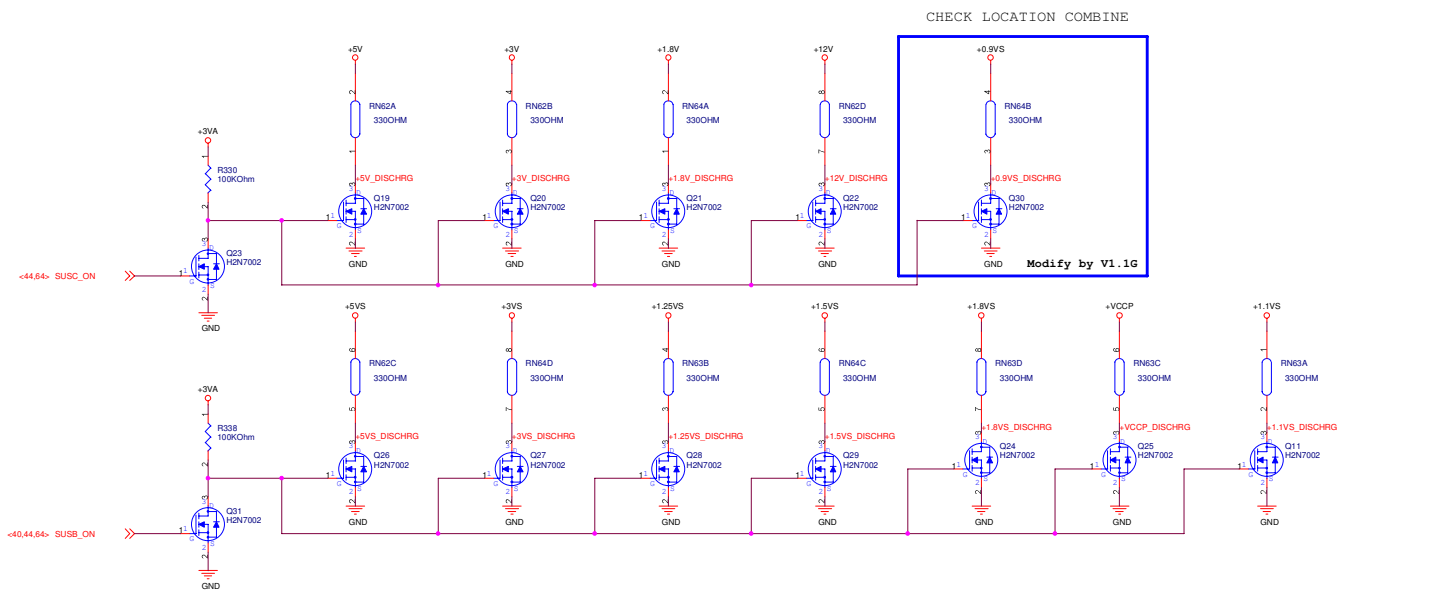
Reserved R to +3VSUS for
Wake up function!



1.1		ASUS		Title : Mini Card	
ASUSTek Computer INC.		Engineer: Alan Chen			
Size	Project Name			Rev	
Custom	Z96S			2.5	
Date: 10/21/2011	Sheet	31	of	65	

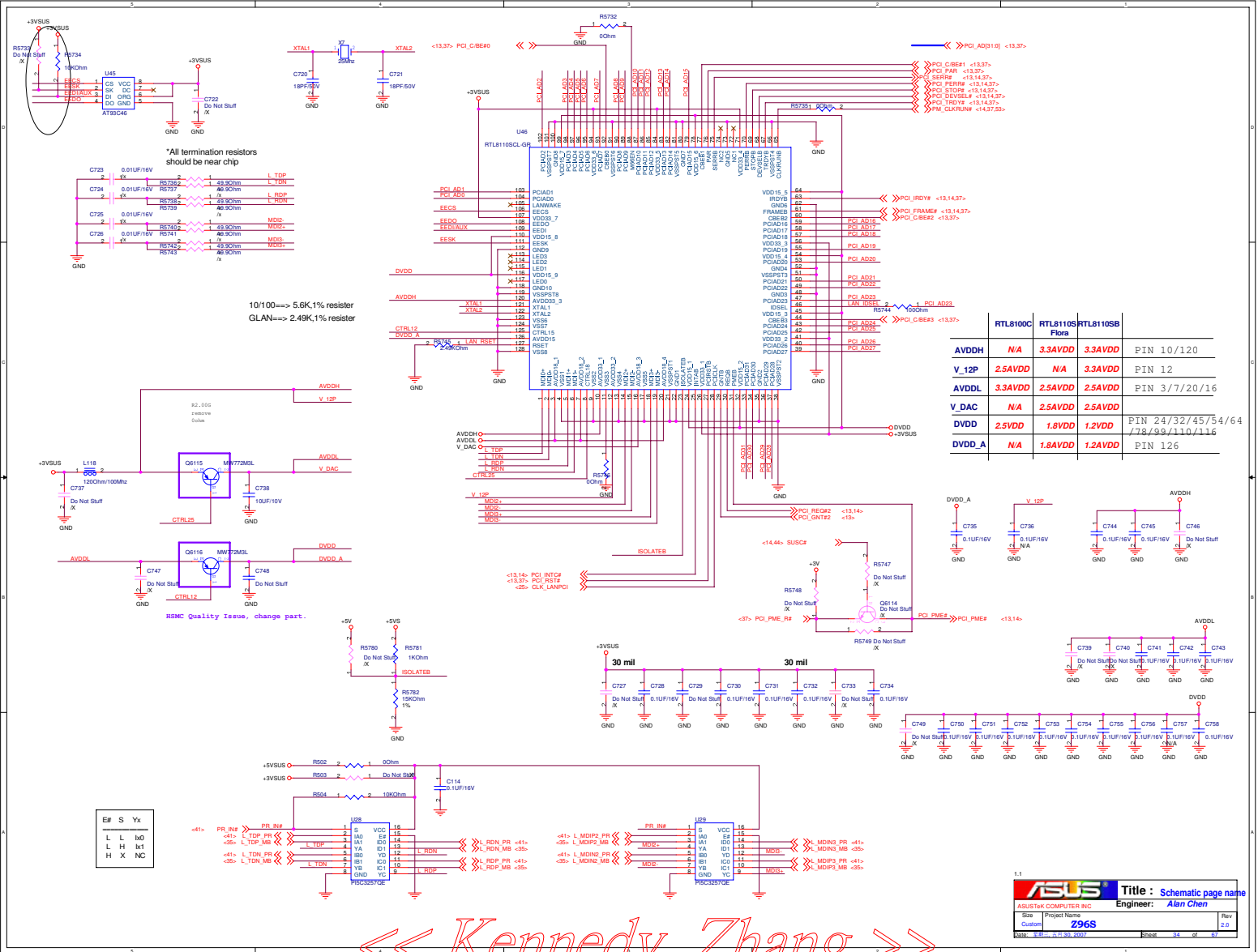
<< Kennedy_Zhang >>

<< Kennedy_Zhang >>

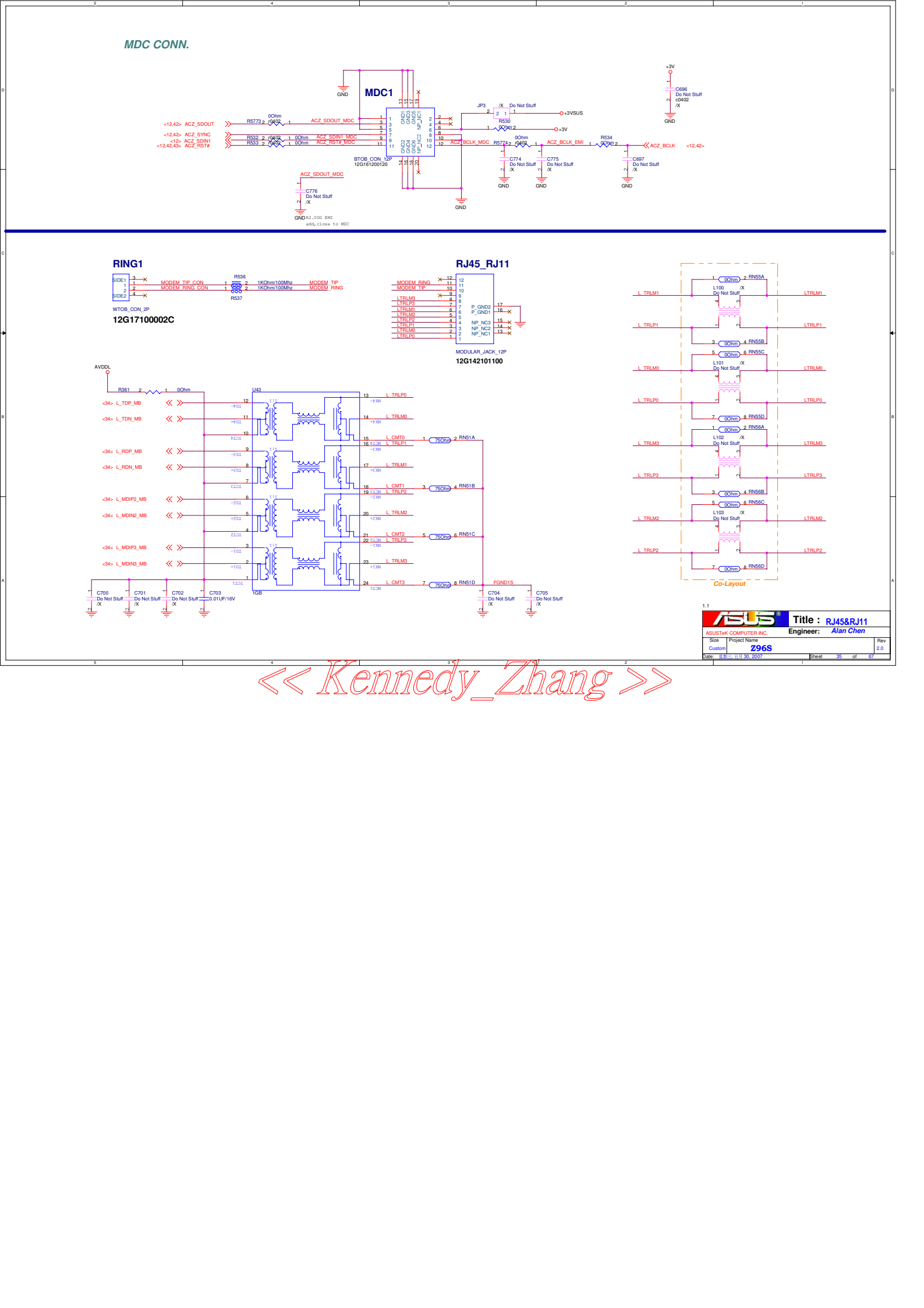
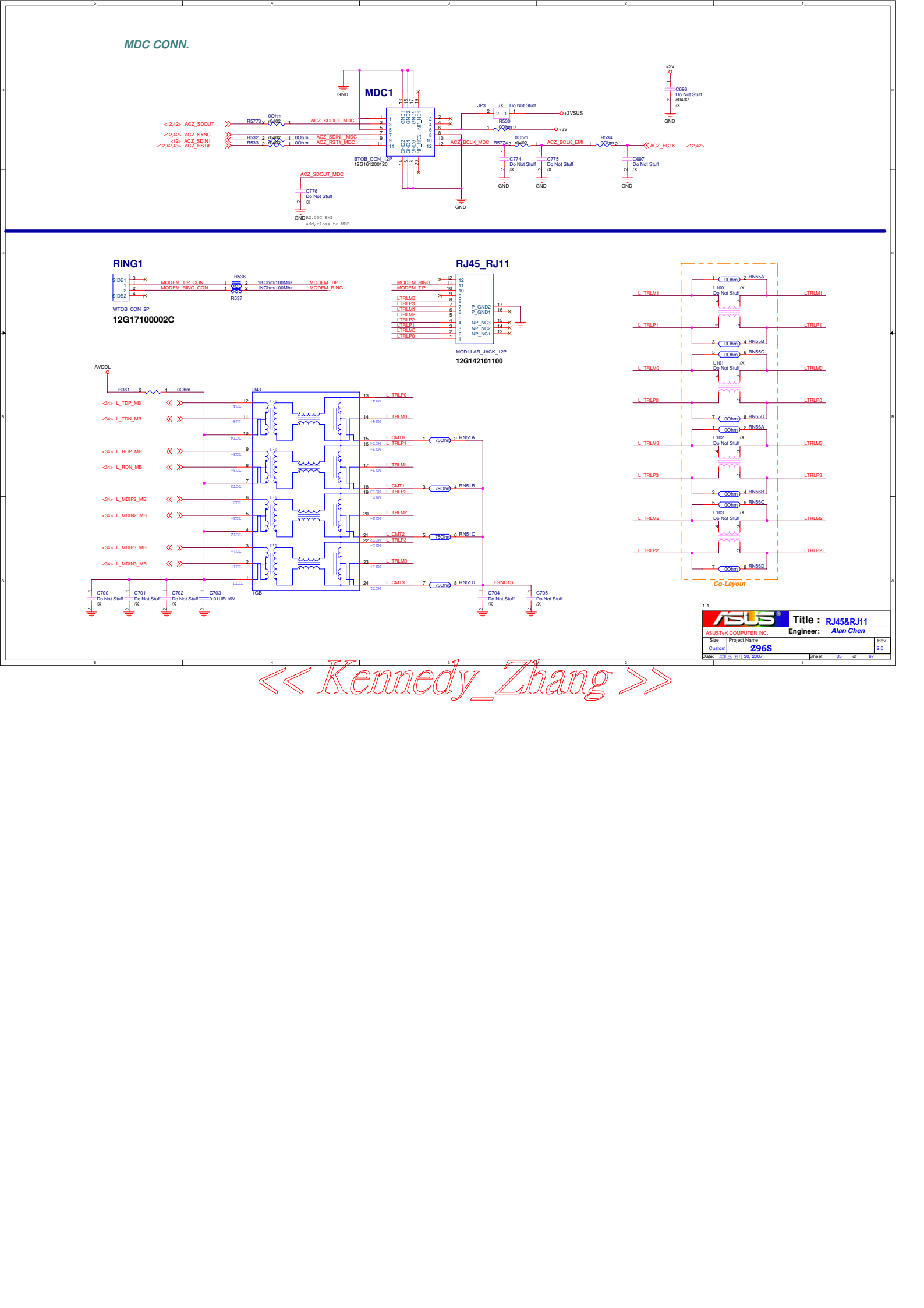
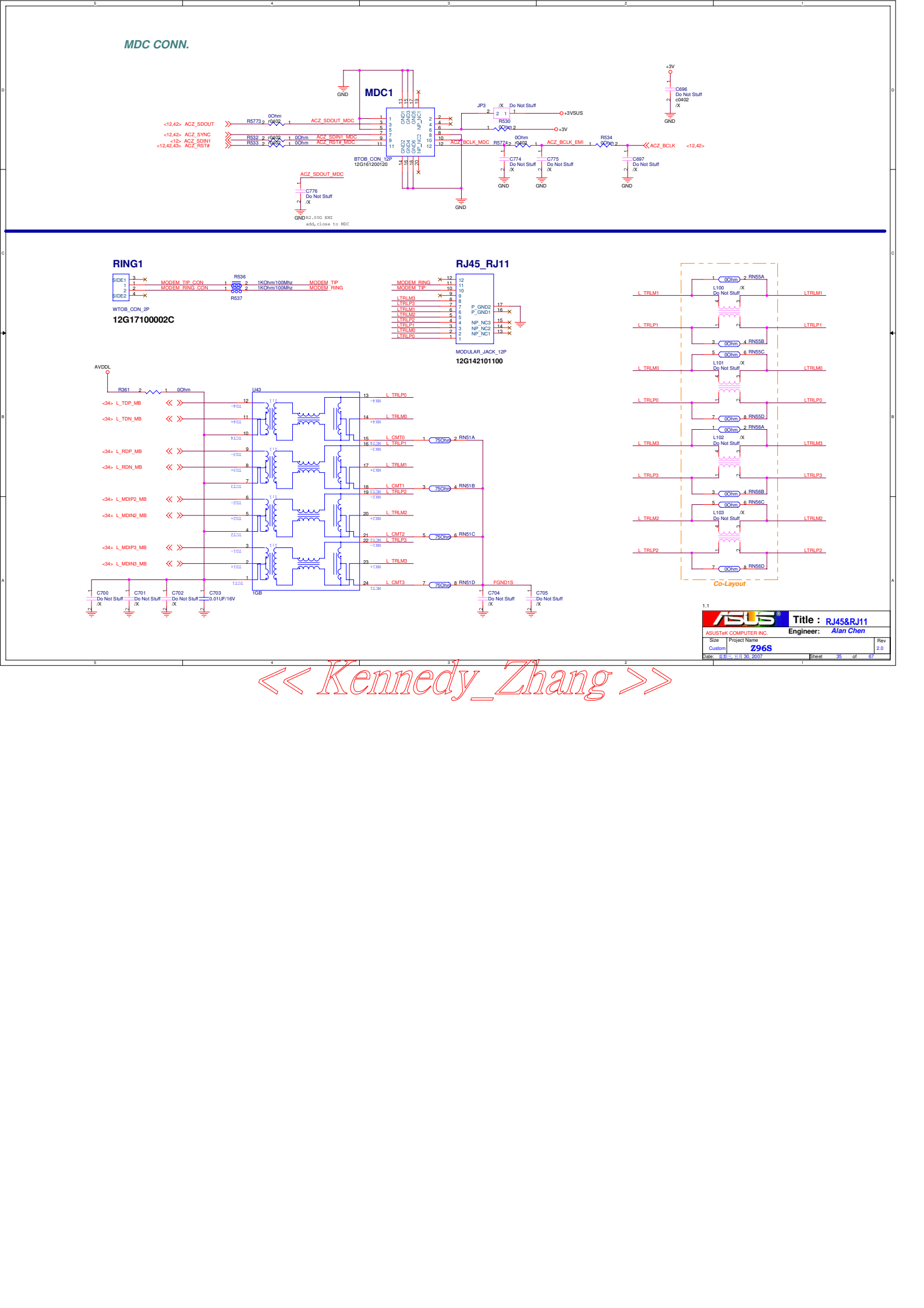
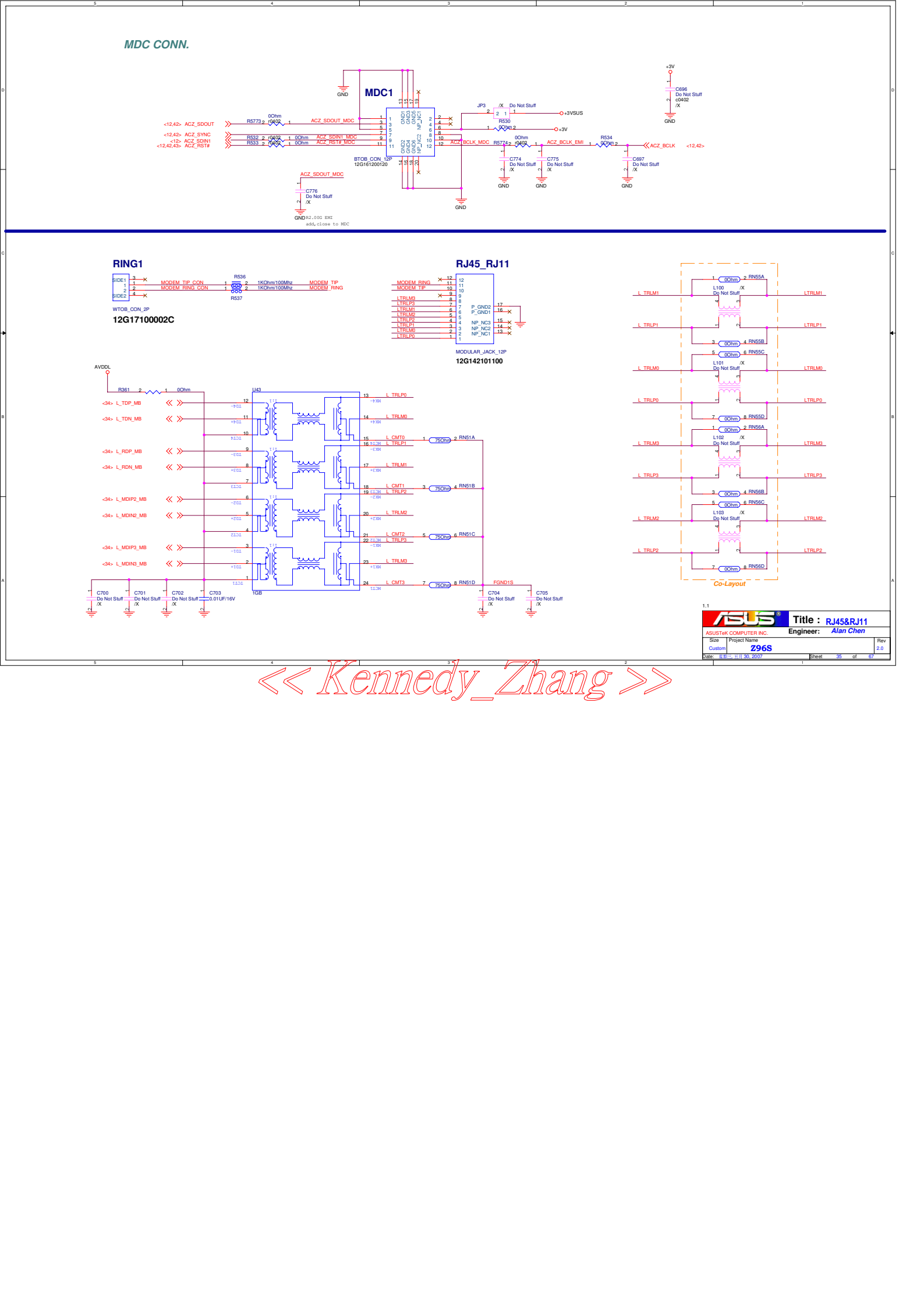


1.1		ASUS		Title : DISCHARGE & EMI CAP	
ASUSTeK COMPUTER INC. NB1		Engineer: Alan Chen			
Size	Project Name			Rev	
Custom	Z96S			2.0	
Date: 10/10/2007		Sheet: 69 of 69			

<< Kennedy_Zhang >>



<< Kennedy_Zhang >>



MDC1

RING1

RJ45_RJ11

Co-Layout

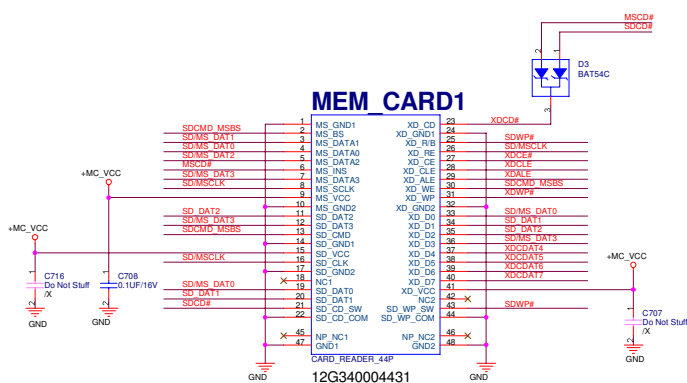
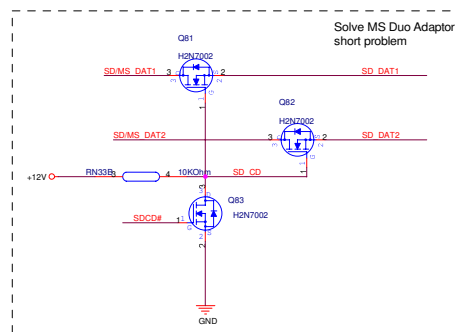
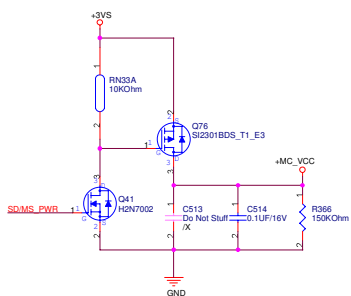
ASUS Title : RJ45&RJ11
 ASUSTeK COMPUTER INC. Engineer: Alan Chen
 Size Project Name
 Custom Z96S
 Date: 11/13/2007 Sheet 35 of 37

« Kennedy_Zhang »



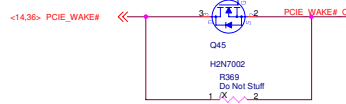
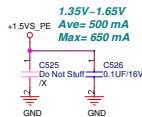
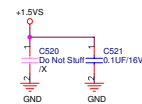
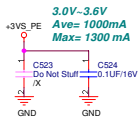
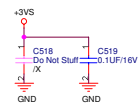
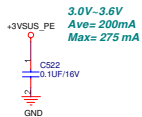
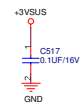
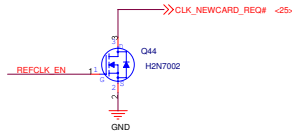
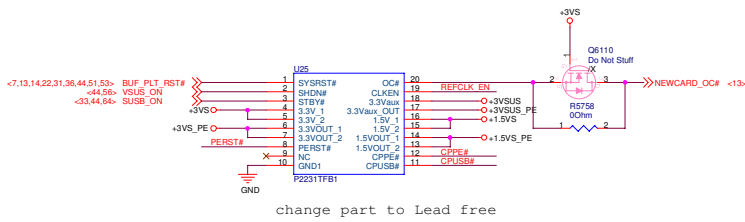
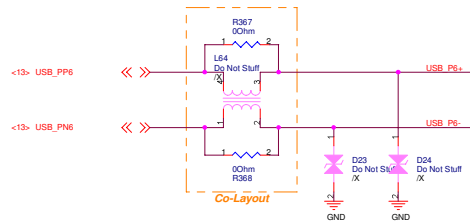
<< Kennedy_Zhang >>

<<XDCDAT7 <3>
 <<XDCDAT6 <3>
 <<XDCDAT5 <3>
 <<XDCDAT4 <3>
 <<SDIMS_DAT3 <3>
 <<SDIMS_DAT2 <3>
 <<SDIMS_DAT1 <3>
 <<SDIMS_DAT0 <3>
 <<SDCMD_MSBS <3>
 <<XDWP# <3>
 <<XDALE <3>
 <<XDCE# <3>
 <<SDWP# <3>
 <<SDCD# <3>
 <<MSCD# <3>
 <<SDMSCLK <3>
 <<SDMS_PWR <3>

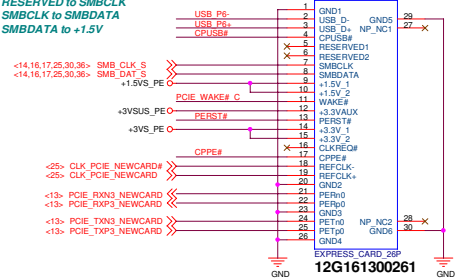


ASUS		Title 3 in 1 CARD READER	
ASUSTek COMPUTER INC		Engineer: Alan Chen	
Size	Project Name	Rev	
Custom	Z96S	2.0	
Date: 2007.10.30	Sheet 39 of 67		

<< Kennedy_Zhang >>



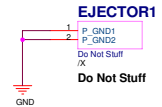
!! ExpressCard Standard 1.0:
Change Pin7 from RESERVED to SMBCLK
Change Pin8 from SMBCLK to SMBDATA
Change Pin9 from SMBDATA to +1.5V



NewCard Header

EXPRESS1

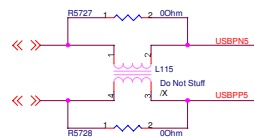
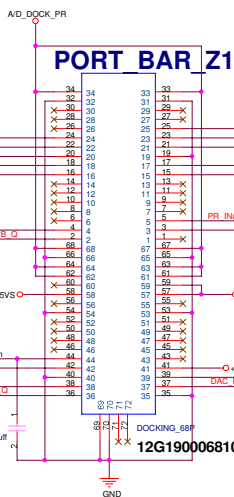
NewCard Ejecter



1.1

ASUS		Title : NEWCARD	
ASUSTek COMPUTER INC. NB1		Engineer: Alan Chen	
Size	Project Name		Rev
Custom	Z96S		2.0
Date: 11/13/2007		Sheet 40 of 87	

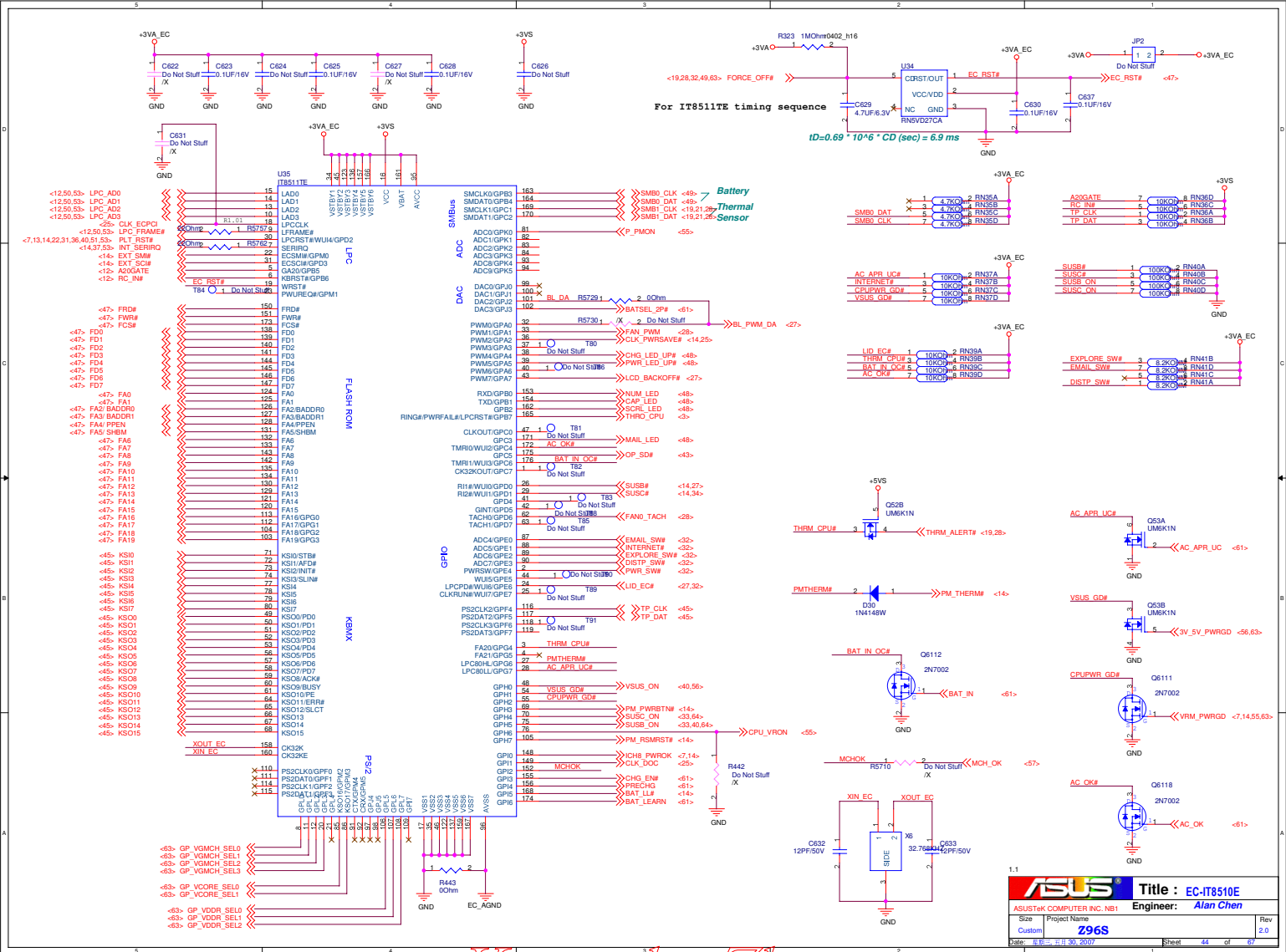
<< Kennedy_Zhang >>



1.1

		Title : <Title>	
ASUSTek COMPUTER INC		Engineer: <i>Alan Chen</i>	
Size Custom	Project Name Z96S		Rev 2.0
Date 2007-07-30	Sheet 41	of 67	

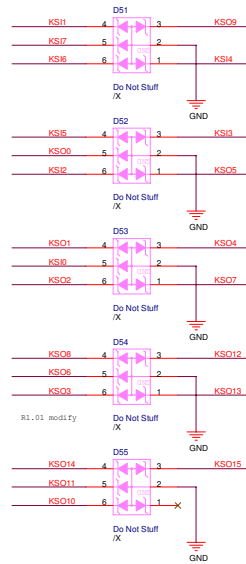
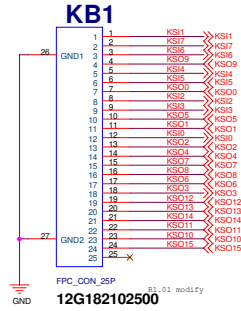
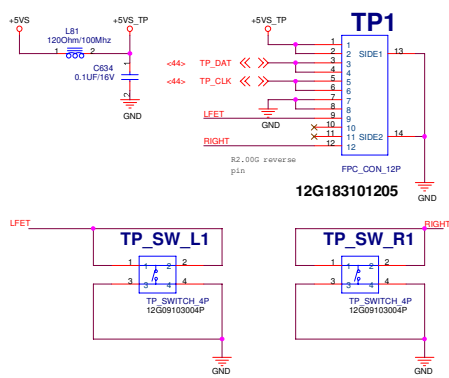
<< Kennedy_Zhang >>



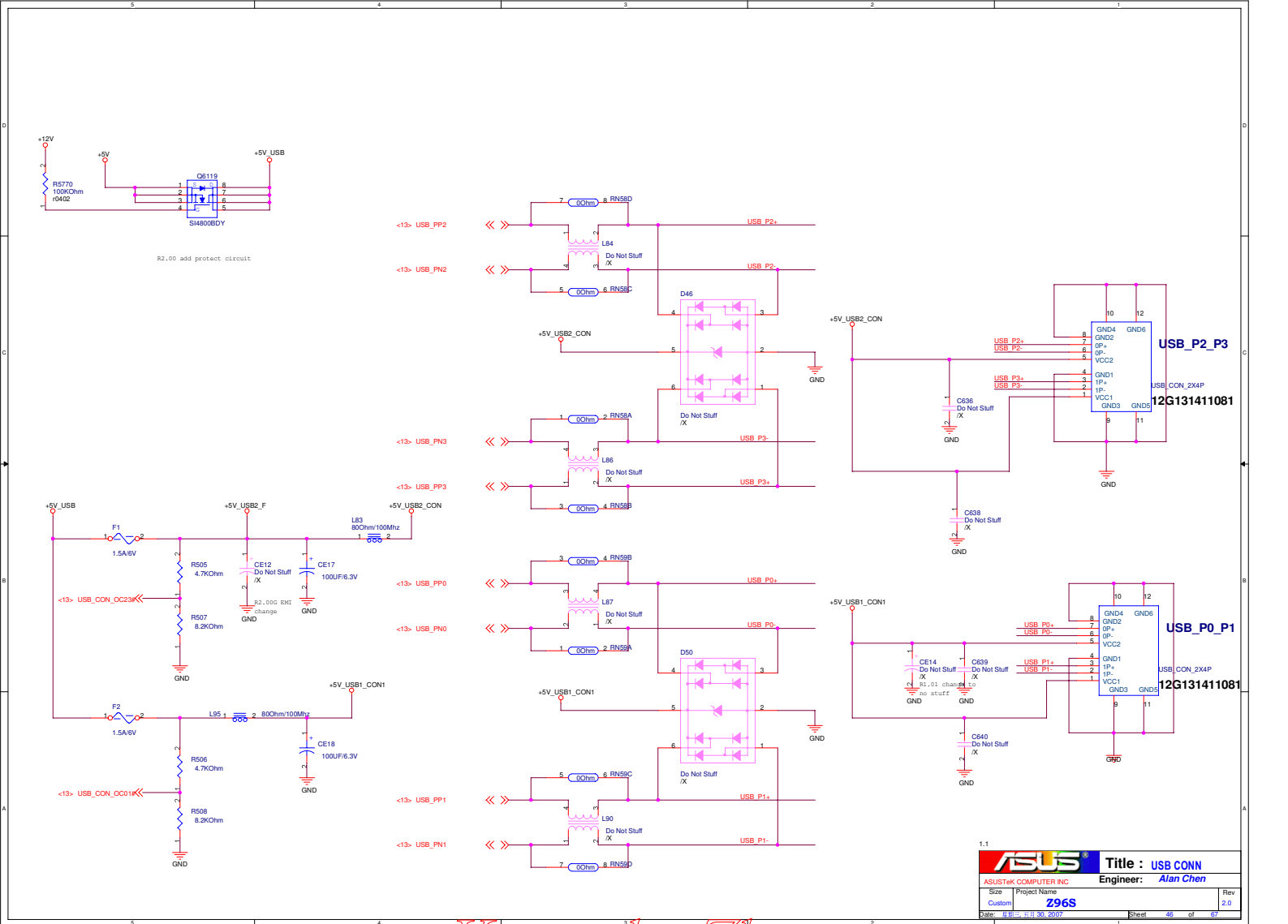
<< Kennedy_Zhang >>

For Touch-Pad

For Keyboard



<< Kennedy_Zhang >>



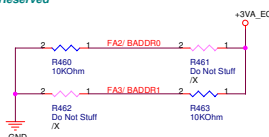
<< Kennedy_Zhang >>

ASUS		Title : USB CONN	
ASUSTeK COMPUTER INC		Engineer: Alan Chen	
Size	Project Name	Rev	
Custom	Z96S	2.0	
Date: 11/13/2007	Sheet 46 of 87		

EC Hardware Strapping

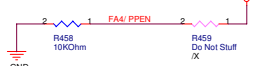
FA2/ BADDR0 & FA3/ BADDR1

00: PNPCNG Access Register Pair Are 002Eh and 002Fh
10: PNPCNG Access Register Pair Are 004Eh and 004Fh
01: PNPCNG Access Register Pair Are Determined by
EC Domain Registers SWCBALR and SWCBAHR.
11: Reserved



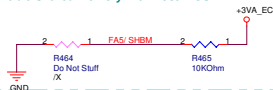
FA4/ PPEN

0: Normal
1: KBS Interface Pins Are Switched to Parallel Port
Interface for In-System Programming

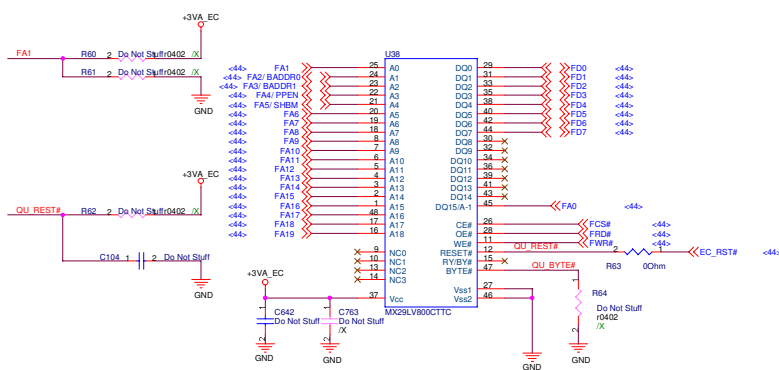


FA5/ SHBM

0: Disable Shared Memory with Host BIOS
1: Enable Shared Memory with Host BIOS



Note: Sampled at VSTBY Power Up Reset



BIOS: 05G001204043

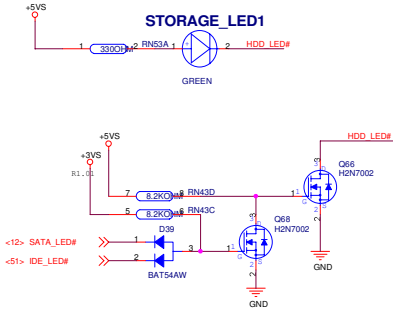
1.1

ASUS		Title :ISA ROM	
ASUSTek COMPUTER INC. NB1		Engineer: Alan Chen	
Size	Project Name		Rev
Custom	Z96S		2.0
Date: 11/13/2007		Sheet 47 of 87	

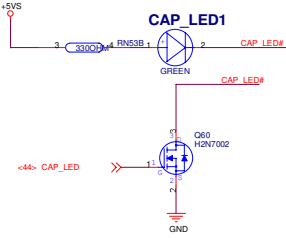
<< Kennedy_Zhang >>

For LED

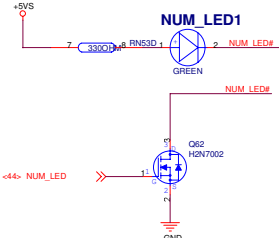
For SATA/IDE LED



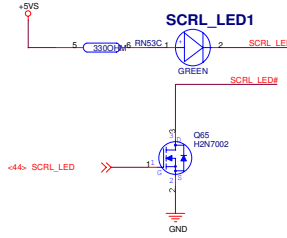
for Cap. Lock



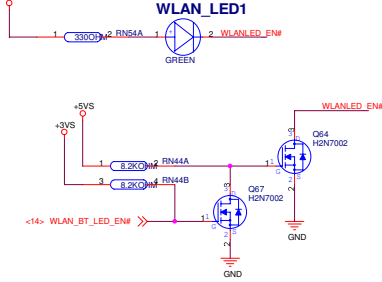
for Num Lock



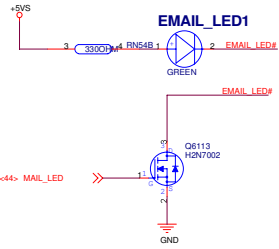
for Scroll Lock



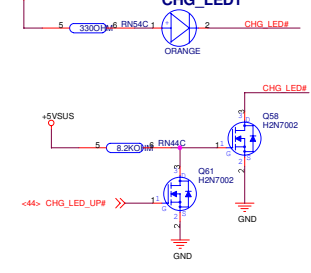
For WireLess LED



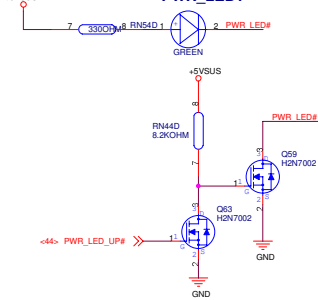
for email



For BATTERY LED



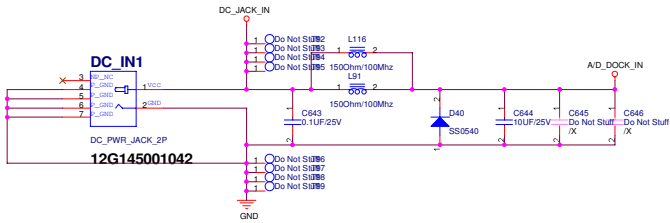
For POWER LED



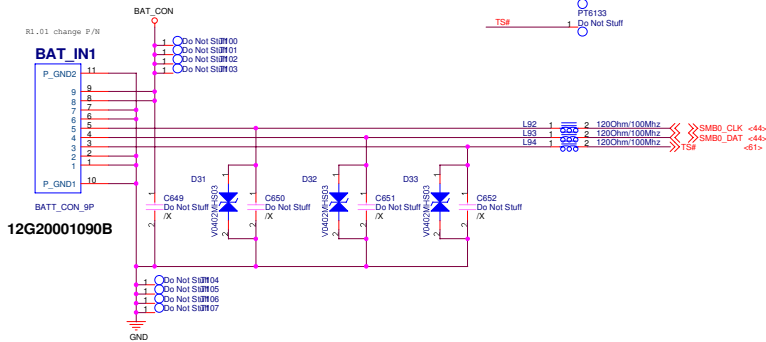
1.1		ASUS®		Title : LED	
ASUSTek COMPUTER INC		Project Name		Engineer: Alan Chen	
Size	Custom	Z96S		Rev	
Date: 11/13/2007		Sheet 48 of 87		2.0	

<< Kennedy_Zhang >>

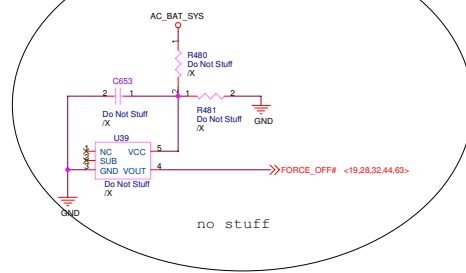
DC IN



BAT IN



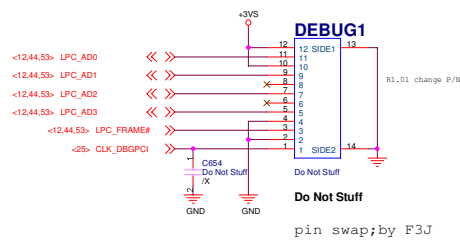
Without Battery & Pull out Adapter



1.1		ASUS®		Title : DC & BAT IN	
ASUSTek COMPUTER INC. NB1		Engineer: Alan Chen			
Size	Project Name			Rev	
Custom	Z96S			2.0	
Date: 11/13/2007		Sheet 49 of 87			

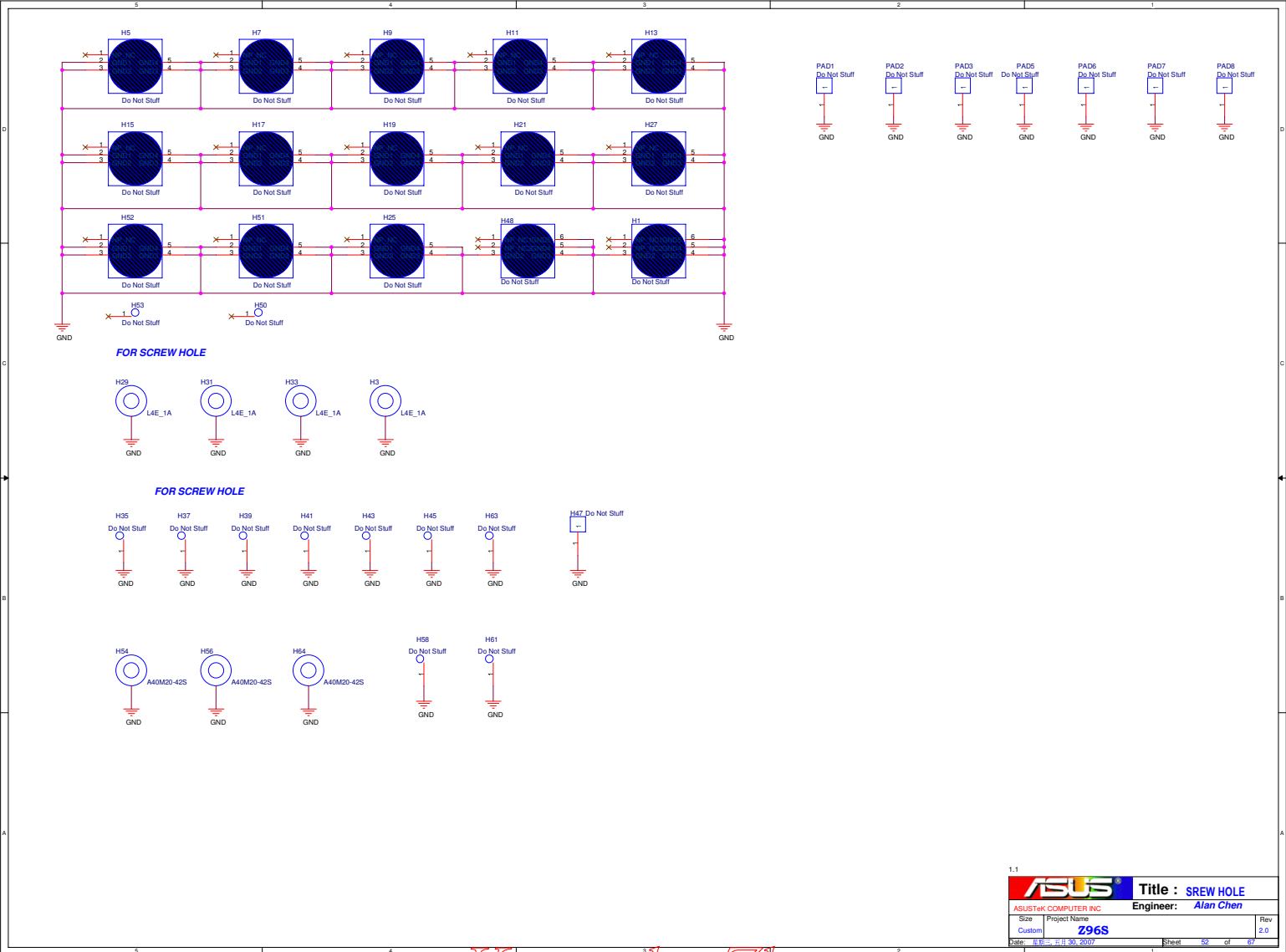
<< Kennedy_Zhang >>

For Debug



1.1		ASUS		Title : Debug CONN.	
ASUSTeK COMPUTER INC.		Engineer: Alan Chen			
Size	Project Name			Rev	
Custom	Z96S			2.0	
Date: 10/10/2007		Sheet: 50		of 67	

<< Kennedy_Zhang >>



<< Kennedy_Zhang >>

1.1		ASUS®		Title : SREW HOLE	
ASUSTek COMPUTER INC		Engineer: Alan Chen			
Size	Project Name			Rev	
Custom	Z96S			2.0	
Date: 11/11/2007			Sheet 66 of 67		

For TPM Module

TPM1

12G16080020J

Pin 6: +3VA
Pin 13: SMB_CLK
Pin 14: SMB_DAT
But R1F removes these three pins to reduce pin number!

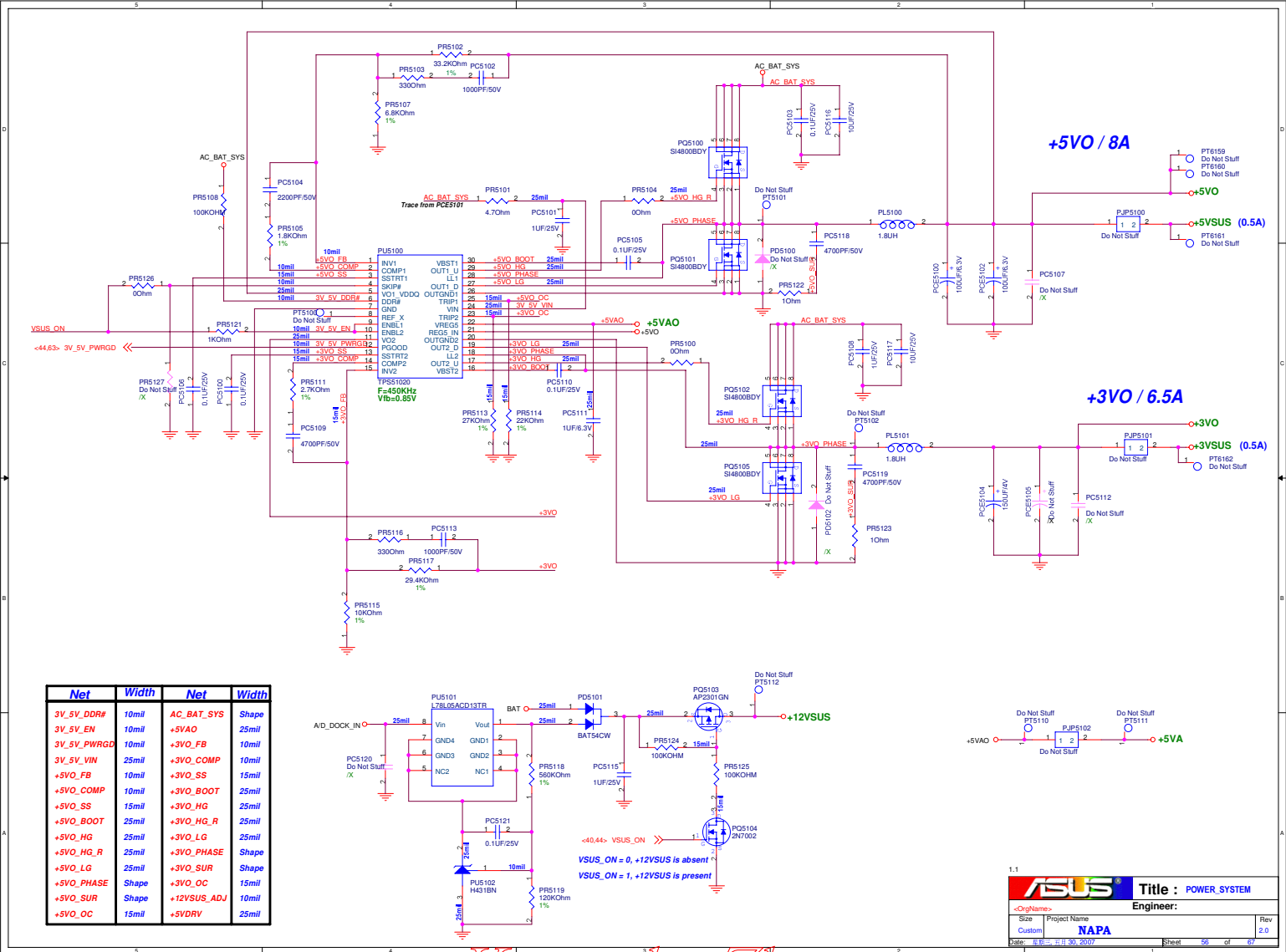
ASUS
ASUSTek COMPUTER INC.
Size: Custom
Date: 08/03/2007

Project Name: Z96S
Rev: 2.0
Sheet: 53 of 67

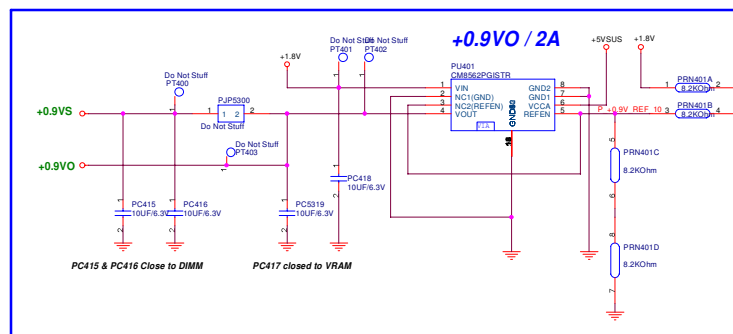
Title: TPM
Engineer: Alan Chen

<< Kennedy_Zhang >>

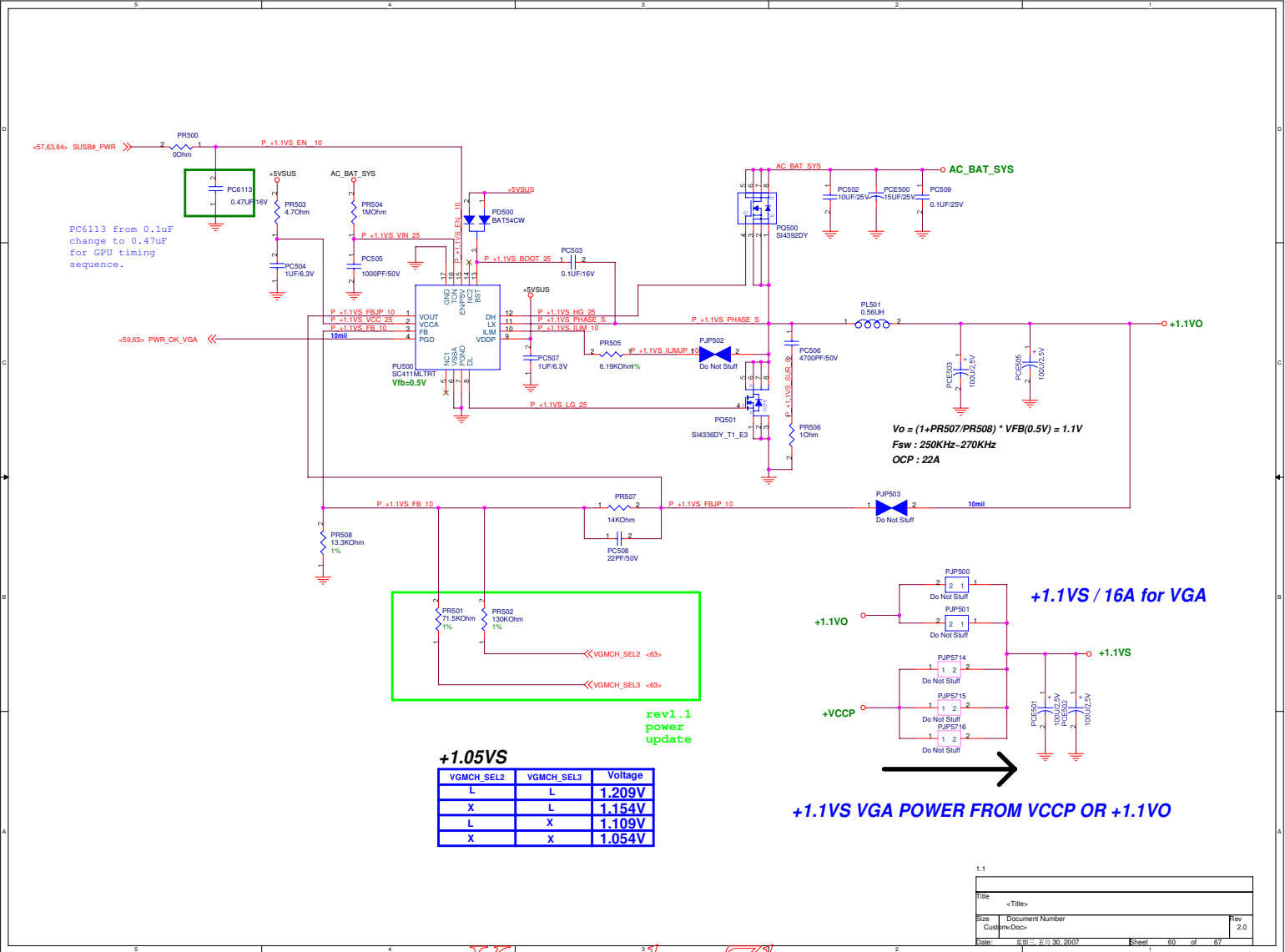




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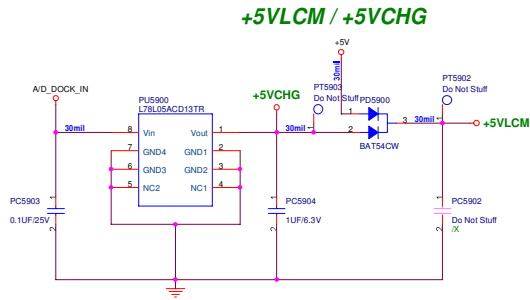
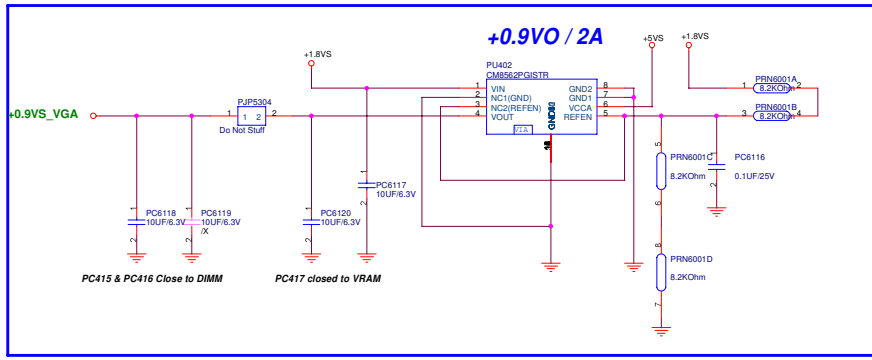


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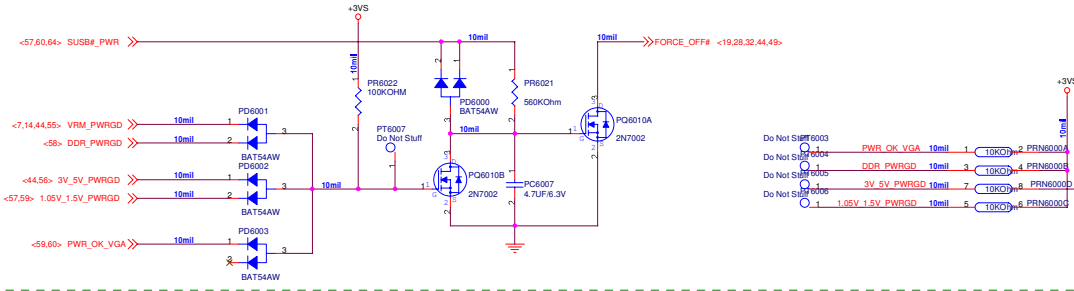
<< Kennedy_Zhang >>



1.1		ASUS		Title : POWER_DETECT	
<OrigName>		Engineer:		Rev	
Size	Project Name	NAPA		2.0	
Custom					
Date: 11/15/2007		Sheet 62 of 67			

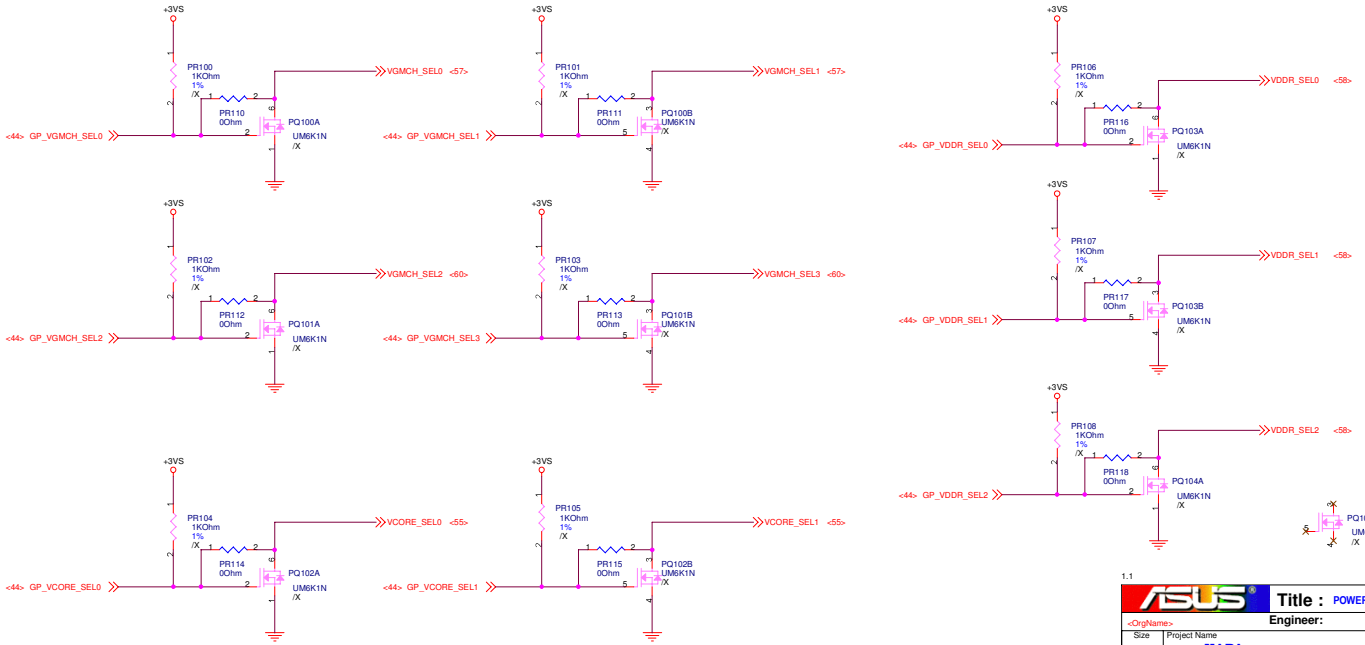
<< Kennedy_Zhang >>

Power Good Detector



Power Voltage control

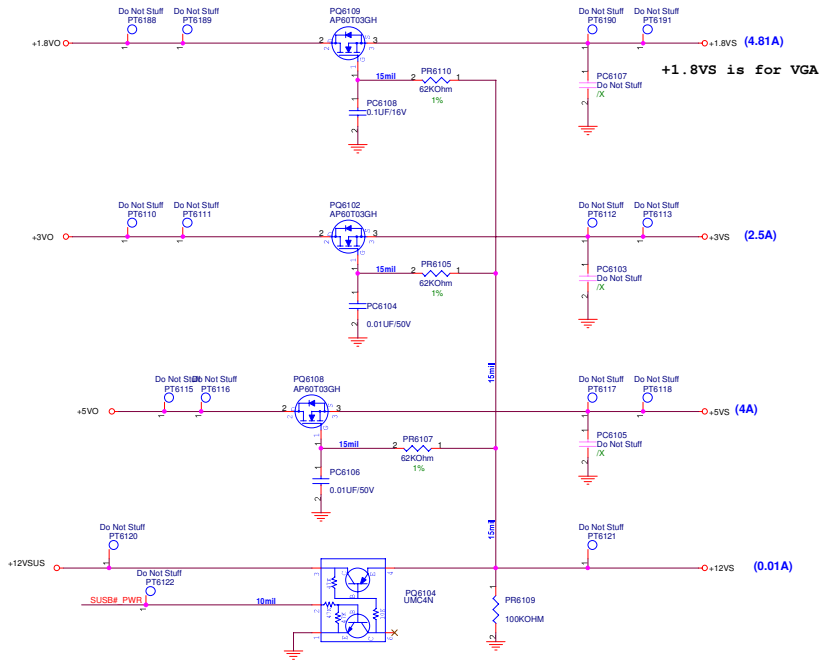
Modify V2.0G



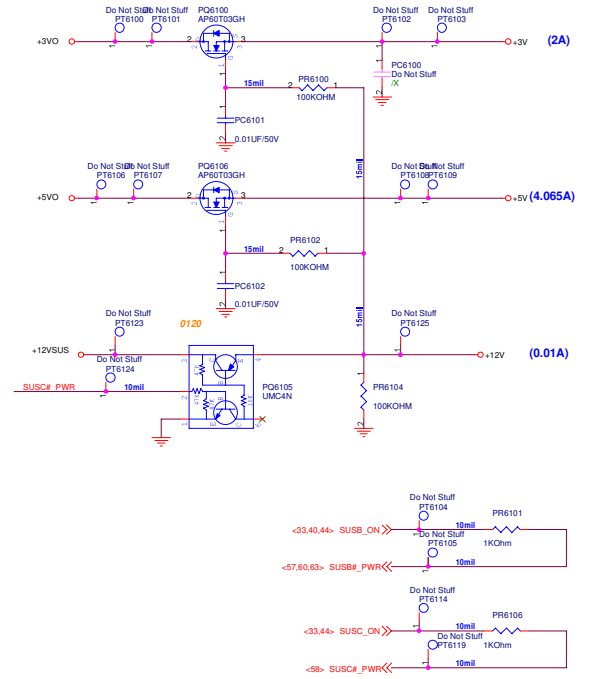
1.1		Title : POWER_PROTECT	
ASUS		Engineer:	
.<OrgName>			
Size	Project Name	Rev	
Custom	NAPA	2.0	
Date: 龙和云, 五月 30, 2007		Sheet	63 of 67

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SUSB#_PWR POWER



SUSC#_PWR POWER



ASUS		Title : POWER_LOAD_SWITCH	
Size	Project Name	Engineer:	Rev
Custom	NAPA		2.0
Date: 11/13/2007	Sheet: 64	of	67

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1.1		ASUS®		Title : POWER_SIGNAL	
<OrigName>		Engineer: Alan Chen			
Size	Project Name			Rev	
Custom	NAPA			2.0	
Date: 11/11/2007		Sheet	66	of	67

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